Session 1 Overview

Plenary Session

Chair: Anantha Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA
ISSCC Conference Chair

Co-Chair: Kevin Zhang
Intel, Hillsboro, Oregon
ISSCC International Technical-Program Chair

The Plenary Session begins with welcome remarks and an introduction from the Conference Chair, Anantha Chandrakasan. Then Kevin Zhang, the Technical Program Chair, will give a brief summary of the 2016 Technical Program. The Plenary Session features four keynote speakers, leaders in their respective fields and collectively represent a broad spectrum of our industry. An Awards Ceremony which recognizes major technical and professional accomplishments, presented by the IEEE, Solid-State-Circuits Society (SSCS), and ISSCC, will take place between the keynote addresses.

William M. Holt, Intel Executive Vice-President and General Manager of its Technology and Manufacturing Group, will provide his perspectives on the semiconductor industry's guiding principal, Moore's Law, its past, present, and future. With growing scaling difficulties and increasing doubts over the vitality of Moore's Law going forward, Holt will directly address these challenges and the opportunities facing our industry. He will use examples of the latest 14nm products to illustrate the benefits of technology scaling and explore innovative devices that will help extend Moore's Law well into the future.

The Internet of Everything (IoE) is broadly considered to be the new frontier for semiconductors and is projected to become a multi-trillion-dollar business by 2020. Sophie V. Vandebroek, CTO of Xerox, will present three foundational elements for future developments in electronics – the "Three Pillars" of IoE, smart everyday objects, information-centric networks, and automated real-time insights. In her talk, Vandebroek will explore how each of these pillars is reliant on microelectronics. Broad applications of IoE will be illustrated through examples from health care to transportation, along with unique challenges and opportunities for integrated circuit and system design.

Mobile communications have been a major growth engine for the semiconductor industry over the past decade. LTE has now become mainstream for mobile technologies. What's next? Seizo Onoe, Executive Vice-President and CTO of NTT DoCoMo, will discuss the future of mobile communications – 5G and beyond. The projection of 5G as a global reality is rapidly accelerating, driven by the need for cellular systems that can provide more cost-effective solutions with wider coverage with broader bandwidth. Onoe will share his views on the history of the evolution of mobile systems, discussing the growth of the definition of 5G and of its technology requirements.

The automotive industry is experiencing a technological revolution largely driven by underlying microelectronics. Cars are rapidly becoming personalized mobile-information hubs, and soon cars will be able to operate autonomously. For this future, connectivity is increasingly essential. Las Reger, CTO of Automotive at NXP Semiconductors, will present the road ahead for securely-connected cars, including vehicle-to-everything (V2X) communications, affordable compact radar detection, and Ethernet for high-bandwidth in-car data transfer. High-bandwidth and reliable wireless technologies along with private and secure systems will be at the heart of future mobile technologies for the automotive industry.

Overall, the Plenary Session will cover a broad range of topics, from the foundations of semiconductor technology to a wide range of future applications in IoE, mobile communications, and automotive transportation. We are fortunate to have four leaders from various sectors of industry to share their insights on the future of integrated circuits and systems at ISSCC 2016. We hope that you will find this Session both exciting and rewarding. Enjoy!

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FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 Moore's Law: A Path Forward **8:45 AM**

William M. Holt, *Executive Vice-President and General Manager, Technology and Manufacturing Group, Intel Corporation, Hillsboro, Oregon*

Moore's Law has served as the guiding principle for the semiconductor industry for 50 years. But now there are growing concerns and doubts over the vitality of Moore's Law going forward, given the scaling challenges we face. This talk will directly address those concerns and explore future opportunities for the industry. We will present the scaling benefits for power, performance, and cost using specific product and design examples based on state-of-the-art 14nm CMOS technology, for applications ranging from high-performance computing down to ultra-low-power mobile applications. In additional to the scaling path of CMOS technology beyond 14nm, this talk will also discuss some leading technology options on the horizon beyond CMOS and their potential design benefits in advancing Moore's Law well into the future. Novel 3D heterogeneous integration schemes and new memory technologies will be discussed for their potential in optimizing the memory hierarchy and addressing bandwidth challenges in processor performance and power.

1.2 Three Pillars Enabling the Internet of Everything: Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights **9:20 AM**

Sophie V. Vandebroek, *Chief Technology Officer, Xerox Corporation, Norwalk, CT*

When smart everyday objects, information-centric networks, and automated real-time insights work in concert a "perfect storm" of functionality emerges, one which will disrupt entire industries: Gartner predicts that the global economic value of the Internet of Everything (IoE) will be $1.7T in 2020. But, even more important will be the inevitable improvements to human society that IoE enables: personalized healthcare and education, agile urban mobility, efficient energy usage, and much more.

This talk will provide examples of how each of the three pillars of IoE relies on electronics: (1) printed hybrid logic and sensor circuits using organic inks and inks embedding microchips to create smart 2D labels and to manufacture 3D personalized Internet-connected objects; (2) information-centric network protocols and hardware (for example, CCNx®) to increase the Internet's versatility, reduce its traffic congestion, improve security, and simplify application development; and (3) machine-intelligence software and deep-learning chips to create real-time insights and automate processes at the "edge" of the IoE network.

The three pillars of IoE will be illustrated through examples from healthcare and transportation. A number of unique challenges and opportunities for general-purpose and custom chip designs will be highlighted.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM**

BREAK **10:20 AM**

1.3 The Evolution of 5G Mobile Technology Toward 2020 and Beyond **10:45 AM**

Seizo Onoe, *Executive Vice President and CTO, NTT DOCOMO, Tokyo, Japan*

Recently, LTE has become the mainstream of mobile technologies; correspondingly, global expectations for 5G are rapidly growing toward 2020 and beyond. Up to the generation of 4G, a representative technology for each generation emerged immediately after the commercial launch of the previous one; However, today, while everyone talks about 5G, there is no single technology representing it. Although researchers see some saturation in the evolution of radio, combinations of existing technologies will continue to create new possibilities and solutions. Thus, through such combinations, developments that are considered impossible today will be achieved in the 5G era. For example, cellular systems will provide cost-effective solutions with wide coverage at even higher frequencies with broader bandwidth. In this talk, the history of mobile-system evolution up to 5G will be reviewed. Then discussion will turn to 5G definition, its requirements, its technologies, and their coverage for variable use cases and spectrum bands. Finally, DOCOMO's recent R&D activities targeting a 5G commercial launch in 2020 will be described.

1.4 The Road Ahead for Securely Connected Cars **11:15 AM**

Lars Reger, *CTO Automotive, NXP Semiconductors, Hamburg, Germany*

The car is evolving: It is transforming from simply a mode of transport to a mobile personalized-information hub! Cars are enabling consumers to seamlessly integrate their mobile and wearable devices, and soon they will be able to operate autonomously.

The technologies that make autonomous driving a reality are clearly on the rise; they include secure vehicle-to-everything (V2X) communications, affordable compact radar detection, and Ethernet for high-bandwidth in-car data transfer.

As well, self-driving cars will integrate a variety of wireless interfaces for exchanging data with other vehicles and the surrounding intelligent traffic infrastructure – all aimed at understanding the world around to optimize the traffic flow, reduce CO2 emissions, and avoid accidents. While providing an essential element of autonomous driving, this connectivity also exposes cars to vulnerabilities such as hackers and viruses.

Powerful reliable wireless technologies combined with the highest-level privacy and system security are critical. This talk will discuss what it takes to realize the secure connected car of the future.

PRESENTATION TO PLENARY SPEAKERS **11:50 AM**

CONCLUSION **11:55 AM**

1.1 Moore's Law: A Path Going Forward

William M. Holt

Executive Vice President, General Manager,
Technology and Manufacturing Group, Intel, Hillsboro, Oregon

1. Moore's Law Guides the Semiconductor Industry

Moore's Law has served as the guiding principle for the semiconductor industry for 50 years. The societal impact brought about by continually increasing the capability, affordability, and availability of integrated circuits is astonishing. Increasing computing power, increasing energy efficiency, and decreasing size of ICs have revolutionized existing industries and enabled new ones. While concerns over the future of Moore's Law have been present from the beginning, the challenges have changed over time. Currently, the challenges of scaling and increasing cost are the focus of concerns and doubts over the vitality of Moore's Law going forward. However, the industry continues to drive progress on many fronts. Continued advances in CMOS technology such as the introduction of 3D transistors provide increasing capabilities over a broader range of use. Novel 3D-heterogeneous-integration schemes and novel package technologies will further extend product benefits. At the same time, new memory technologies provide opportunities to fundamentally change memory hierarchy and bandwidth to resolve challenges in processor performance and power. In addition to the scaling of CMOS technology beyond 14nm, there are leading technology options on the horizon beyond CMOS with potential design benefits that can advance Moore's Law well into the future.

2. Economics is the Driving Factor

In 2015, Gordon Moore reflected on his 1965 paper, "The message I was trying to get across was that integrated circuits were the road to less-expensive electronics. It really evolved from being a measure of what goes on in the industry to something that more or less drives the industry." [1] Fundamental driving factors of Moore's Law are cost and capability. The drivers to enhance capability have changed over time as focus changed from DRAM to high-performance processing to power efficiency and lower-power SoCs, but the need to be cost effective remains.

Cost-per-transistor is an effective way to measure cost while accounting for differences in features. Cost-per-transistor can be determined by multiplying cost-per-area by area-per-transistor as shown in Figure 1.1.1 [2]. Cost-per-area has increased with successive technology generations; most recently, this increase has accelerated. Cost increases are driven by the need for more-complex processing, more-advanced tools, and increased numbers of process steps required to achieve the feature size as well as to incorporate new materials and architectures to achieve performance and energy-efficiency goals. In order to offset these cost increases, corresponding increases in density are required. Recently, higher-than-historical-density increases have been achieved through architectural innovations (such as 3D transistors) and implementing design rule and process improvements (such as multi-patterning lithography). This density acceleration has enabled the continuation of the historical cost-per-transistor reduction trend as shown in Figure 1.1.1. The resulting decreases in cost-per-transistor can be allocated as cost reduction or as capability increase, depending on the targeted application.

Technology-node timing has also been discussed in the context of Moore's Law. The timing of node introduction has not been uniform over the history of Moore's Law, with some node introductions earlier and some later [3]. In the 1970s, the interval between node introductions was commonly three years, then varying from one to five years prior to a concerted effort in the 1990s to achieve a two-year cycle. In addition, node conversion and technology introductions have not been simultaneous across the industry. While node timing will continue to vary, the driving force for node introduction continues to be the ability to deliver higher capability and better power performance cost effectively over time.

3. Silicon Technology Scaling

Transistor scaling continues to provide higher performance, lower power, and lower cost-per-transistor. Comparing an Intel® Core™ i5 processor on Intel's 14nm process to the 4004, the first commercially available microprocessor, shows a 3,500× increase in performance, 90,000× increase in energy efficiency, and 60,000× decrease in price per transistor [4].

Innovations in process and devices have been essential to continuing Moore's Law as shown in Figure 1.1.2 [5]. Process technology has implemented continual transitions from bipolar to MOSFETs, to CMOS to voltage scaling, to power-efficient scaling, and to System-on-Chip design. Significant processing innovations in CMOS include tungsten plugs, trench isolation, CMP (chemical mechanical polishing), copper interconnects, strained silicon, high-κ/metal gates and FinFETs. The introduction of strained silicon improved drive current. High-κ/metal gates reduced current leakage and heat. FinFETs addressed limitations of electrostatics and short-channel effects.

A snapshot of current silicon-technology scaling can been seen using Intel's 14nm process as an example. The 14nm process incorporates second-generation FinFETs, air-gapped interconnects, self-aligned double patterning, and a 0.05μm^2 SRAM cell size. Figure 1.1.3 shows the improvement in PMOS I_{dsat} and I_{dlin} for Intel's 14nm technology node compared to that for 22nm. Note that I_{dsat} is improved 15% for NMOS and 41% for PMOS over 22nm. Air gaps at critical performance layers provide a 17% improvement in capacitance. A thick top metal is used for improved on-die power distribution. Fin pitch, a key measure of transistor density for FinFETs, is scaled to 42nm, maintaining the historical 0.7× scaling trend from 22nm [6] [7].

While there are many measures of the improved capability that advancing technology provides, possibly the most important is the trend in improving power efficiency. This can be best seen by graphing energy times delay (CV^2 * CV/I = C^2V^3/I) over several generations. Figure 1.1.4 shows improvements in power efficiency with successive generations. Scaled process technologies provide a combination of higher performance and lower power.

An example of how this translates into the product can be seen with Core™ M and fifth generation of Core™ processors on 14nm process technology (code named Broadwell). Over a 2× reduction in total dissipated power (TDP), 60 to 80% higher graphics performance and a 60% reduction in SoC idle power versus the 4th generation Core™ product was achieved using key design optimizations and capabilities provided by the new process technology [8].

4. Scaling of Analog Circuits, Mixed-Signal Circuits, and SRAMs

Despite a general trend toward making integrated analog components more "digital", high-quality analog features must be maintained in scaled CMOS process nodes. Traditionally analog components such as PLLs, I/Os, and thermal sensors have gradually converted some analog functions to digital as the power and area cost of logic has reduced with scaling. But most of these digitally-assisted analog architectures still rely on high-quality analog building blocks such as linear amplifiers, DACs, and regulators. As an example, within Intel's 22nm and 14nm technology nodes, transistors and passives were engineered to maintain or improve analog capability while dramatically scaling analog area. The conversion to a FinFET architecture reversed the trend of degrading transistor intrinsic gain (g_m*r_o) and V_t variation starting in 22nm and continuing into 14nm as shown in Figure 1.1.5 [6]. The 14nm semi-digital delay-locked loop described in [9] illustrates how selecting a co-optimized combination of core analog components (delay line, regulator, R-C filter, etc.) along with digital control and calibration, results in better performance, power, and area at scaled process nodes.

In some ways, blocks that are considered traditionally "analog" such as serial I/Os, push the process performance harder than the CPU core or memory. Per-pin I/O data rates double about every four years to keep pace with aggregate system bandwidth requirements [10]. By contrast, microprocessor clock rates have increased relatively slowly over the past decade, instead, emphasis has been on more-power-efficient parallel architectures. As a result, today's serial I/O pin rates such as 8Gb/s PCIe Gen3 or 25Gb/s Ethernet now far outpace the core clock rate. Even the transfer rate of memory interfaces such as DDR will exceed the core frequency within a few years. As shown by [11] and [12] (Figures 1.1.6, 1.1.7), high-speed interfaces continue to benefit from process scaling in terms of density and power. Designing high-speed interfaces in scaled processes clearly requires careful consideration of layout effects within the transistors and interconnect stack. But the continued improvement in area density and power is essential to keep pace with aggregate system bandwidth requirements, which are growing even faster than per-pin bandwidth [12].

SRAM remains the workhorse as the embedded memory for all VLSI applications. Continuous voltage scaling for power efficiency has created a significant challenge in SRAM design to achieve lower operating voltage. The minimum operating voltage of SRAMs is directly determined by the variation

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control of underlying transistor technologies. Because of the significant improvement in transistor variation in the most advanced 14nm FinFET [6], a much improved SRAM V_{CCmin} has been achieved as shown in Figure 1.1.8 [7].

5. Memory and 3D Integration

Memory has always been an essential component of high-performance energy-efficient computing across entire platforms. To offset fundamental limitations of various memory technologies, memory hierarchy was established to address the overall system-level memory needs (as shown in Figure 1.1.9 [13]. The hierarchy often consists of on-die SRAM as high-speed cache memory, off-chip DRAM as main memory, and high-density NAND as storage, supplemented by a hard-disk drive. But, with ever-increasing demand for memory bandwidth to support new applications, such as high-resolution graphics and cloud computing, the traditional memory solution is no longer sufficient. Recently, in-package memory has proven to be an effective solution to bring high-memory bandwidth (>100MB/s) directly to compute engines [14]. Various memory technologies, including enhanced DRAMs and logic-based high-performance eDRAMs, have been used to serve as the memory core. Currently, a technology breakthrough in high-density nonvolatile memory, called 3D XPoint™ [13], will provide a new way forward in terms of memory-hierarchy optimization, as this technology has blurred the traditional boundary between memory and storage with DRAM-like speed and NAND-like density. Accordingly, a system-level optimization will be needed to take full advantage of new memory technologies moving forward.

While monolithic integration driven by Moore's Law continues to provide the fundamental path to achieve higher performance and lower cost, in-package and 3D integration can also assist in providing a good balance in achieving performance and size improvements for various applications. 3D die-stacking has now been widely adopted by memory manufacturers as an economical solution to achieve high memory density. But logic-to-logic and/or logic-to-memory integration still remains an open field. Silicon interposers have been explored to provide multi-chip integration where data bandwidth is crucial. However, the cost overhead of the conventional silicon interposer scheme has been rather prohibitive for broad adoption of this technology. A new chip-level integration scheme, Embedded Multi-chip Interconnect Bridge (EMIB) shown in Figure 1.1.10 [15], has been developed to provide a much improved cost-performance trade-off. In this approach, a tiny silicon bridge is embedded in the package substrate to provide a dense chip-to-chip interconnect for high data bandwidth while keeping the cost adder to a minimum.

As new memory technologies emerge and new chip-to-chip and 3D integration schemes are introduced, it will become more important to re-optimize the overall system-level architecture and configurations to achieve optimal performance and economic benefits.

6. Future CMOS Transistor Technologies

Transistors have been the core of Moore's-Law semiconductor technology for over half a century. During this time, the transistor has evolved with technologies over the years, from bipolar to silicon-gate PMOS, through NMOS to CMOS. Recently, the continuing pursuit for better electrostatics has led to a major revolution with the introduction of the 3D transistor or FinFET device. Further improvement can potentially be achieved using a gate-all-around or Si nano-wire structure. The ever-increasing demand for faster switching has also driven the need for better conduction materials, such as Ge-channel for PMOS and III-V channel for NMOS or Ge for both NMOS and PMOS channels [16]. Carbon nanotubes (CNT) and 2D semiconductor materials are showing early potential for transistors. (Figure 1.1.11). However, these are still MOSFET transistors and will eventually be a limiter in how low the supply voltage can scale.

7. Beyond CMOS Devices

New devices that do not depend on traditional carrier transport have emerged over the past fifteen years or so. They have shown early promise as a way to help further advance Moore's Law in the future. Two, worthy of further consideration are the tunnel FETs (TFETs) and spintronic devices.

In order to lower power consumption in future technologies, there is a need to lower supply voltage (V_{DD}) to reduce switching energy (~CV_{DD}^2) while keeping leakage currents low. However, when CMOS supply voltage is scaled aggressively to sub-0.5V, performance suffers significantly since the physics-limited subthreshold slope does not permit scaling of threshold voltage (V_t) without unacceptable increases in leakage. In contrast, the tunnel FET transistor can use steeper subthreshold slopes to lower V_t, thus enabling supply voltage operation lower than that for CMOS.

Since the first few experimental TFETs have demonstrated subthreshold slope (SS) steeper than the MOSFET limit (SS = 60mV/decade at room temperature) [17 to 19], researchers have tried to improve the steepness of SS and increase the TFET on-current. Although TFETs can be built using conventional Si as channel material, Si realizes only a very low on-current and also the steep slope occurs at very low current levels, due to its large indirect bandgap and carrier mass. Thus, III-V materials have attracted interest as a TFET channel option due to improved material suitability (low direct bandgap and low carrier mass). The prospects for TFETs are further improved by using a heterojunction to lower the effective tunneling barrier [20] (Figure 1.1.12). The first experimental sub-60mV/decade SS III-V TFETs were demonstrated in 2011 [19]. Comparison to theory shows that the devices can be improved when scaled by removing parasitic currents and improving electrostatics by using a thin body structure [21].

One of the main challenges of realizing steep-SS TFETs is low defect (trap) density and thin-body geometry requirements. A comprehensive study of TFET geometry and defect effects has been carried out with experimentally-calibrated models [22]. Intrinsic-material band-to-band tunneling properties extracted from the experimental data and body thickness were found to be very critical parameters (Figure 1.1.13). Whereas existing bulk-material quality is found sufficient, oxide interface state density not exceeding $10^{12}cm^{-2}$ is required to realize steep SS. For a Ge TFET with body thickness >20nm, and oxide thickness >1nm, steep-SS is not expected even with an ideal oxide (Figure 1.1.14). Steep SS can be realized only for an aggressively scaled body ~5nm, due to strong double-gate control of the channel.

Comparing future N-TFETs to Si MOSFETs at L_G=13nm for various TFET material options has shown that each TFET has advantages over a MOSFET at different current levels (Figure 1.1.15) [23]. Circuit simulations using atomistic device models of a nanowire with L_G=13nm (ITRS 2018 technology node) were used to compare power-performance of CMOS and TFET logic. The results were also compared after adding the effects of device variation for MOSFETs and TFETs. Due to their steeper I_D-V_G curve characteristic, TFETs are more susceptible to higher leakage-current variation while for the MOSFET drive-current variation is larger. When variations are included, TFET logic still shows 54% better energy-efficiency than CMOS for the same performance (delay=40ps) (Figure 1.1.16). Clearly, there is potential in TFETs, but there also remain challenges that will require innovation for solution. [24]

Another class of beyond CMOS devices [25], is called spintronic logic. These devices use magnetization of a nanoscale ferromagnet to hold the logic state. Some of the device concepts are based on current-controlled switching by spin torque, which is the effect of spin polarized electrons changing magnetization as in Figure 1.1.17. Spintronic devices differ in geometric structure and the way the spin torque switching works: "All-spin" logic [26] utilizes spin-polarized current produced by one nanomagnet to switch the next. In "charge-spin" logic [27] magnetization controls charge current via tunneling magnetoresistance (TMR). This current is used to switch another nanomagnet using the Spin Hall Effect (SHE). Both "domain-wall" logic [28], and "mLogic" [29], are based on the TMR effect, as well, but the charge current moves domain walls with spin torque and thus switches magnetization. "Spin-torque-oscillator" (STO) logic [30] is based on synchronization of phases of STOs.

Other device concepts are based on voltage-controlled switching of magnetization using magnetoelectric (ME) effects. Such effects are, for example, magnetic exchange bias created by an adjacent anti-ferromagnet, change of magnetic anisotropy by strain of an adjacent piezoelectric material, or voltage controlled surface anisotropy as in Figure 1.1.17. In the spin majority gate [31, 32] magnetizations of three inputs are switched by the ME effect, which results in domain walls propagating in ferromagnetic wires. These domain walls compete to determine magnetization direction at a single output. Spin wave devices [33] form a majority gate as well, but the logic states of inputs propagate as spin waves in ferromagnetic wires and switch the nanomagnet at the output.

These new devices have demonstrated excellent potential in addressing many key challenges of conventional scaling, including switching-energy efficiency and leakage power. In general, ME devices have about two orders-of-magnitude smaller switching energy and similar switching delay to that for spin-transfer-

torque devices. However, while magnetoelectric devices have smaller switching energy, they are about two orders-of-magnitude slower in their current form than conventional CMOS at the same technology node [34]. The energy advantage of spintronics stems from the lower switching voltage and the collective nature of switching magnetization rather than numerous individual electrons. As the demand for lower power continues, a place for these devices may emerge.

Another attractive feature of spintronics is that its elements are non-volatile (that is the computation state remains unchanged when the power is switched off). This may open up a new way to architect future computing for a broad range of applications at very low energy, well below that achievable in CMOS.

The experimental realization of many of these spintronic devices has only been demonstrated recently, while others are still in simulation stage. Spintronics is rapidly increasing in its breadth and depth of novel approaches that use magnetism for logic and memory.

These new magnetic devices have demonstrated excellent potential in addressing many key challenges of conventional scaling, including switching-energy efficiency and device-leakage power. While such new devices are encouraging in the search for advancing Moore's Law well beyond the current technology, Si-based CMOS technology will continue to have a significant lead in overall performance and product-level integration. Thus, incremental enhancements in current Si-based technology will likely dominate the mainstream semiconductor industry until new materials and/or devices reach sufficient maturity to meet high-volume manufacturing needs.

8. Conclusion

Semiconductors continue to be the foundation for computing and communications solutions, the basis of the Internet of Everthing, and the primary driver in the future of electronics applications. Moore's Law has led to evermore-powerful smart phones, tablets, personal computers, and data centers. It has enabled computing to become a seamless and powerful force in our homes, offices, cars, factories, and much more. Much has been written about the end of Moore's Law. More recently, speculation has focused on the economic end of Moore's Law. Gordon Moore initially projected 10 years of visibility. [35] Over fifty years later, the Moore's Law horizon remains around 10 years. Moore's Law was never guaranteed. It has thrived and will continue to do so as the result of continuous innovation, rigorous planning, and technology execution. Even though it is getting more expensive to build wafers, improvements in density can provide real cost reduction at the most fundamental level, and this economic benefit drives the ability to continue investing in Moore's Law. Innovations have driven Moore's Law through numerous technological transitions and will continue to power us into the future of CMOS and beyond. As long as there is a cost benefit and rich options for future innovations there is no reason to predict an early end!

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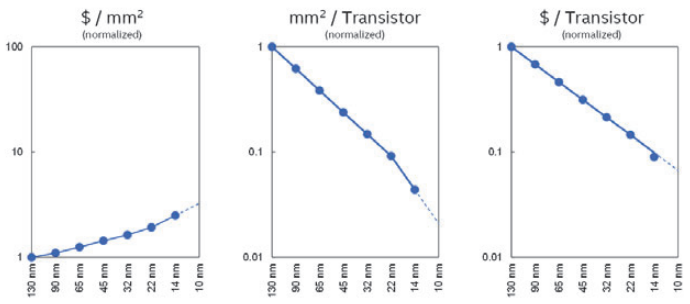

Figure 1.1.1: Cost/Area × Area/Transistor = Cost/Transistor [2].

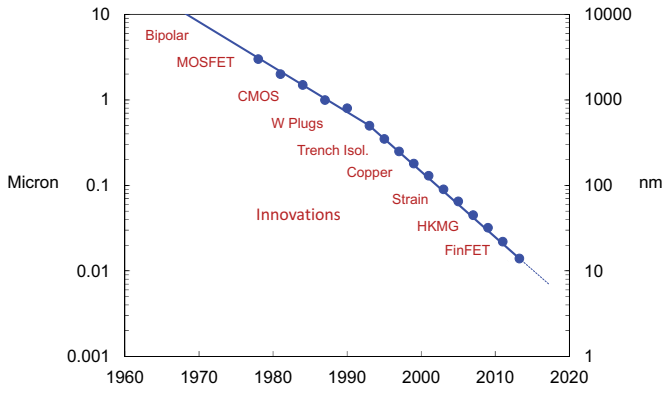

Figure 1.1.2: Process and Device Innovations Essential to Moore's Law [5].

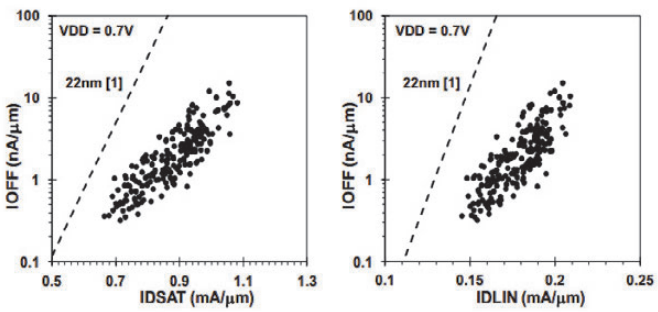

Figure 1.1.3: PMOS I_{dsat} and I_{dlin} curves for 14nm [6].

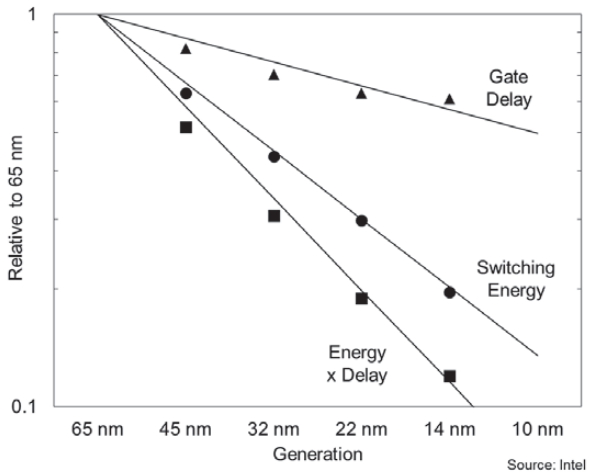

Figure 1.1.4: Generational Technology Benefits.

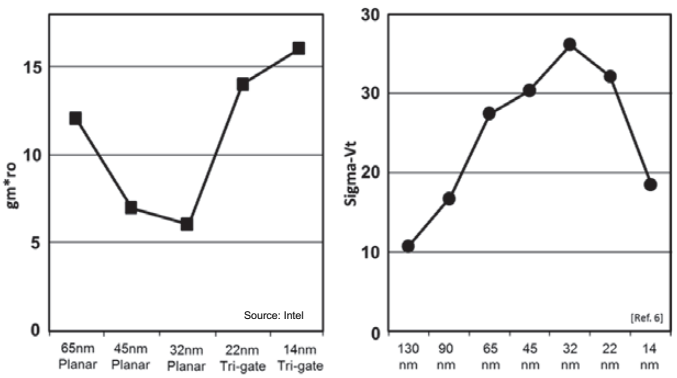

Figure 1.1.5: Intrinsic gain and Sigma-V_t scaling trends through 14nm.

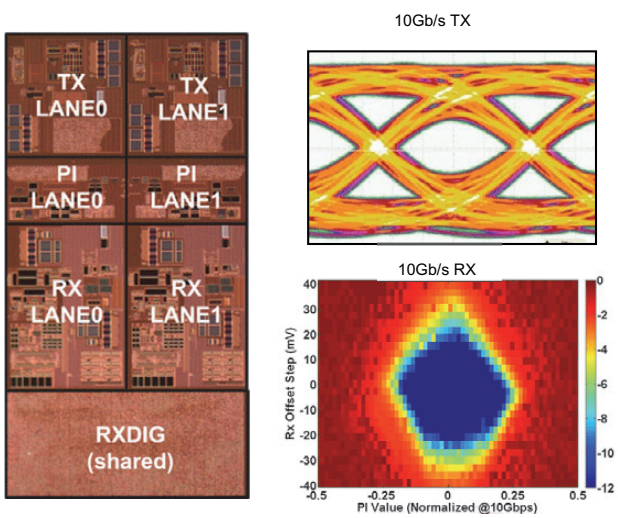

Figure 1.1.6: 10Gb/s serial I/O in 14nm CMOS [11].

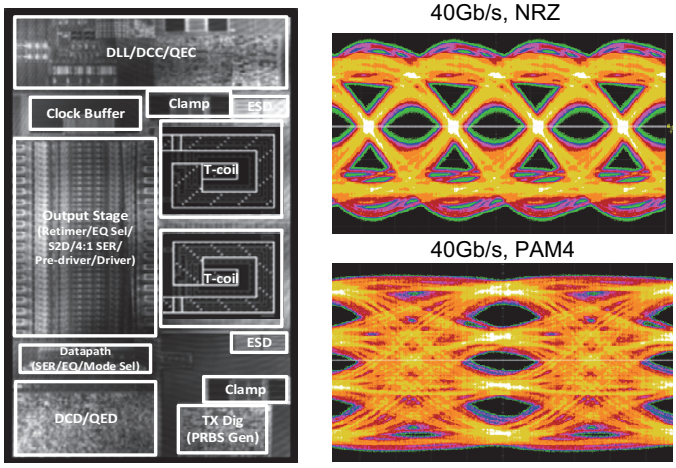

Figure 1.1.7: 16 to 40Gb/s NRZ/PAM4 transmitter in 14nm CMOS [12].

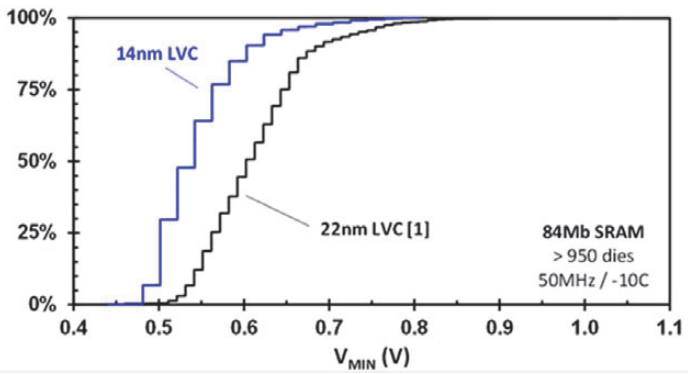

Figure 1.1.8: Improved SRAM V_{CCmin} [7].

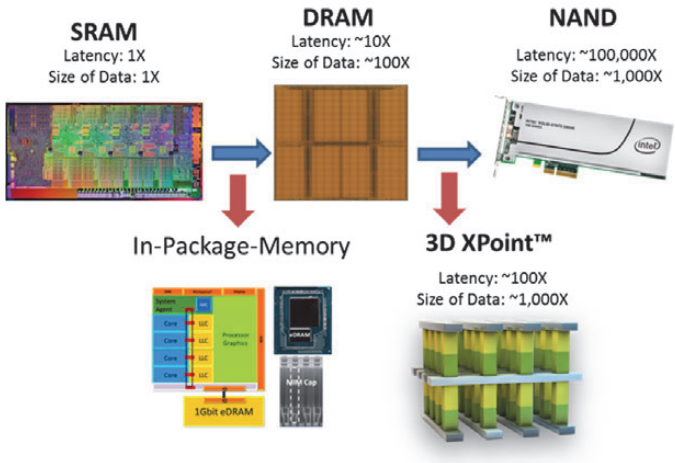

Figure 1.1.9: Memory Hierarchy [13].

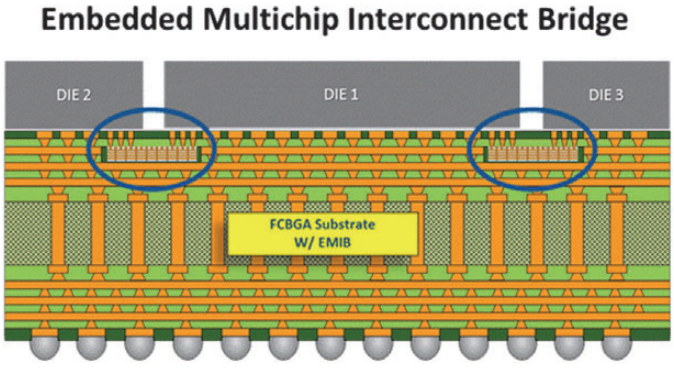

Figure 1.1.10: Embedded Multi-chip Interconnect Bridge (EMIB) [15].

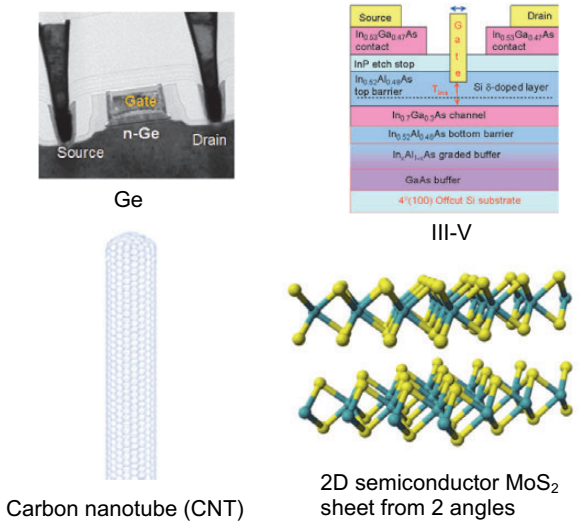

Figure 1.1.11: Transistors with New Materials.

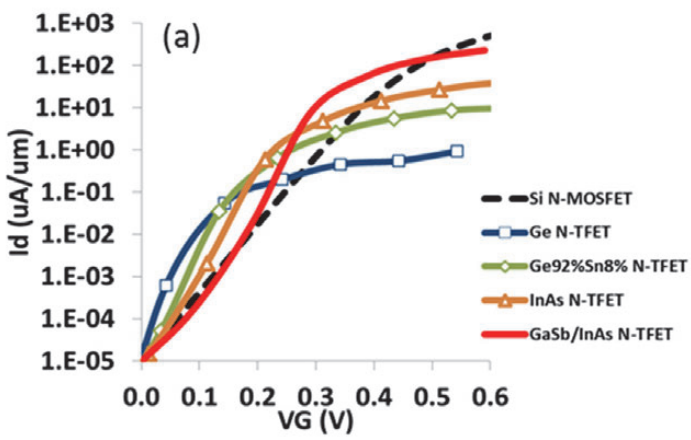

Figure 1.1.12: TFET I_D vs V_{GS} for a range of tunneling junction materials compared to Si MSOFET at L_G=13nm [23].

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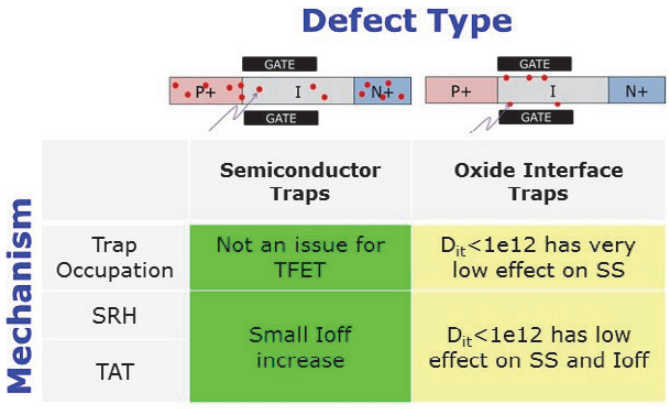

Figure 1.1.13: Summary of possible TFET defects/traps including SRH (Shockley-Read-Hall) and TAT (trap-assist-tunneling) and their impact on the SS I-V performance [22].

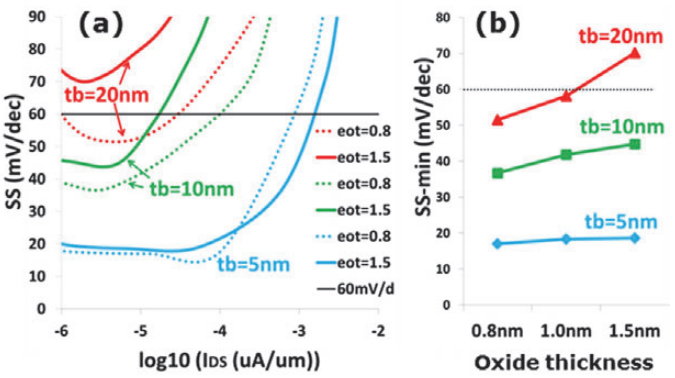

Figure 1.1.14: The effect of Ge TFET geometric dimensions on its SS I-V performance for a long L_G [22].

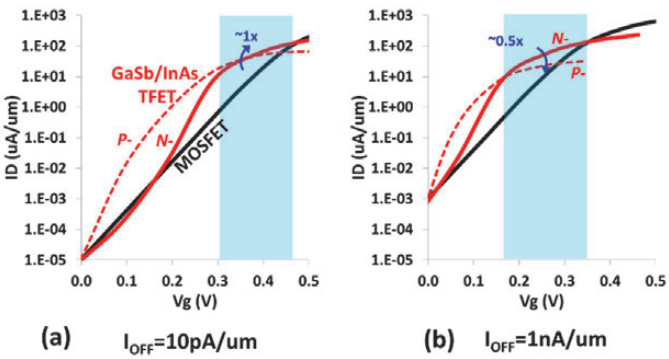

Figure 1.1.15: N-TFET and P-TFET compared to MOSFET devices: I_D vs V_{GS} for two I_{off} targets [23].

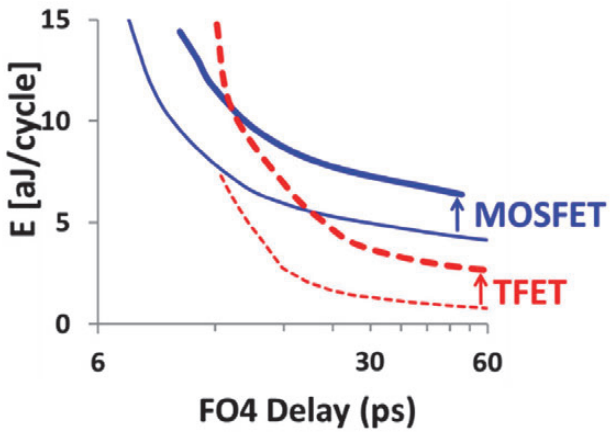

Figure 1.1.16: Energy vs Delay without (thin lines) and with (thick lines) device parameter variations [23].

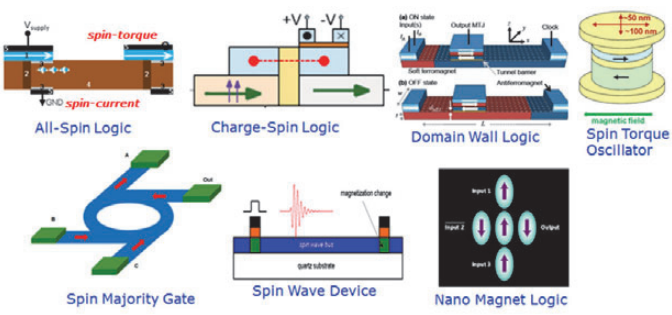

Figure 1.1.17: Schemes for various proposed spintronic logic devices: Spin torque switched devices (top row) and magnetoelectric switched devices (bottom row) [25].

1.2 Three Pillars Enabling the Internet of Everything: *Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights*

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1. Introduction

When smart everyday objects, information-centric networks, and automated real-time insights work in concert, a perfect storm of functionality emerges and the Internet of Everything (IoE), as it is often labelled, is created. Entire industries will be disrupted by the IoE. Businesses and governments will need to comprehend how to surf the transformational IoE waves instead of being swamped by them. The global economic value of the IoE is predicted to be $1.7 Trillion in 2020 [1]. But, more significant will be the positive impact on human society that the IoE will enable: individualized healthcare and education, less urban congestion, efficient energy usage, and much more. This plenary talk will discuss three pillars supporting the IoE and examine how they are enabled by specialty software and electronics.

The first pillar of the IoE consists of the *billions of everyday objects that are becoming smart and connected*: from wearable devices, to food and medicine packaging, to a variety of items in our homes and offices, as well as most industrial machines. These objects are the nodes in the IoE. Xerox has a long history of working on the IoE before it was termed this way: Mark Weiser at PARC coined the term "ubiquitous computing" in the 1980s, which he defined as "technology that is all around us and recedes into the background of our lives" [2]. Correspondingly, for the past 15 years, fleets of printers and multifunction devices connected through the Internet have been remotely serviced. More recently, Xerox's Business Process Outsourcing (BPO) services extended IoE to fleets of cameras for automated tolling, traffic-light applications and parking services, thereby connecting vehicles to civic infrastructure. But, this is just the beginning: It is estimated that 50 billion objects will be connected to the Internet by 2020 [3]. Today, it is traditional silicon electronics that connect objects such as cameras, beacons, wearables, and a variety of other sensors to the Internet. *Printed electronics labels* using organic and inorganic inks are the next opportunity to add intelligence to everyday objects and to make them part of the IoE. Beyond that, researchers are exploring the printing of silicon-plastic hybrid electronics to create three-dimensional objects from scratch. This is accomplished by means of inks containing a variety of microchips in combination with novel additive 3D manufacturing processes.

A second pillar is the emergence of *information-centric networks* that address the security and bandwidth limitations of the current Internet. As the IoE expands, the immense magnitude of unstructured data now flowing through it will explode. The current host-centric or point-to-point network architecture (IP) approach will be inadequate. Novel future Internet architectures using information or content-centric network protocols (such as CCNx®) and specialty networking hardware are under development to address these challenges. This information-centric architecture will increase the Internet's versatility, reduce its traffic congestion, improve its security, and make the creation of applications simpler.

A third pillar consists of the *automated real-time insights* created from the vast amounts of data generated by smart objects and ubiquitous distributed sensors. The IoE will provide a wealth of individualized data on everything: flow of people through cities, patients through hospitals, goods through factories, automobiles through highways, and more. Performing automated real-time analytics in a privacy-preserving and secure way will be essential. When prescriptive analytics are coupled with control systems, a digital nervous system is created that enables automated broad real-world, real-time optimization. For example, Xerox helps drivers find parking spaces, while at the same time assisting city officials with pricing incentives to spread out parking and reduce traffic. Trade-offs will need to be made between performing analytics in the cloud versus processing the data at the edge of the network. Computing at the edge requires extremely low-power and low-cost electronics. As this paper will show, creating automated real-time insights at the IoE edge is enabled by advanced machine intelligence software and emerging deep-learning chips.

These three emerging IoE pillars pose a number of unique challenges and opportunities for general-purpose and custom chip designs. The IoE nodes will require electronics that are extremely low-cost, disappear in the fabric of everyday objects, and perform real-time analytics in a power-efficient and privacy-preserving way. The novel networks will require powerful processors that can not only transfer but also process and store huge amounts of information. These challenges and more are highlighted in this paper. The ISSCC community is ideally positioned to solve them.

2. Smart Everyday Objects

Connecting everyday objects as nodes on the IoE presents several challenges and opportunities. Today, most Internet-connected devices simply resemble a box: they are based on silicon chips and circuit boards, which are housed in an enclosure. But, to be truly successful and become ubiquitous, smart objects will need to be customized and personalized. This requires shaping electronics into unique form factors such that they are compatible with flexible, conformal, large-area, and even soft devices, for example as wearables [4,5] or for other applications shown in Figure 1.2.1. New flexible materials and components as well as novel integration techniques are required to make such electronics robust [6]. For example, flexible thin microchips and compliant interconnects are essential for embedding electronics in everyday objects.

Overall, closer integration of sensors, actuators, microchips, micro-electro-mechanical systems (MEMS), and fluidic devices, at low cost and low power is essential. Toward this goal, printing technologies offer an interesting path for integrating a variety of functions on various novel substrate such as paper or stretchable plastic [7,8]. Conductive inks provide an additive digital solution for interconnects and make it possible to configure on-demand unique electronic circuits. Printed sensors and antennae are in use already in RFID devices [9]. Printed flexible smart labels are the next opportunity to add intelligence to packaging [10]. These require conducting, semiconducting, and insulating inks that can create reliable transistors and other electronic components.

Perhaps the most exciting challenge is to develop new manufacturing approaches for embedding electronics and silicon microchips literally within the fabric of everyday objects. Printing hybrid silicon-plastic circuits, using "functional inks" containing microchips, is an exciting new research direction [11]. Additive 3D manufacturing methods are currently in use not only for prototyping but also for creating actual products for medical, aerospace, and other applications that require individualized parts. Merging 3D printing methods with printed electronics allows the creation of custom 3D smart objects [12]. The key for making "intelligence" a ubiquitous feature of everyday objects is to develop novel integration techniques merging form and function right from the design all the way to the manufacturing processes used in the electronics.

2.1 Conventional Chip Advances and Limitations

Integrated circuits (ICs) have been scaling along the trend of "More Moore" towards 10nm, offering on the way increasing density and lower power consumption. But, beyond 7nm, severe physical limitations are looming. However, packaging advances in 2.5D and 3D offer some possibility for further integration by stacking dies. A trend for smart systems has been the "More than Moore" functional diversification where various types of components such as analog, digital, power, memory, and sensor are combined as a System in a Package (SiP). This trend has been identified by the International Electronics Manufacturing Initiative (iNEMI) and the International Technology Roadmap for Semiconductors (ITRS) as a solution for systems that are interacting with people and the environment [13].

Tighter integration and miniaturization of systems increasingly requires handling bare dice. Furthermore, in order to create thinner packages or chip stacks, dice must get thinner. But, in addition to saving space, thin silicon chips also enable flexible robust electronics that can bend with mm radius [14]. Currently, flexible microchips such as microcontrollers and analog-to-digital converters are being commercialized by American Semiconductor Inc. [15] (Figure 1.2.2) among others. As well, ultrathin devices are being explored as "electronic tattoos" on skin for medical applications by companies such as MC10 [16]. Thin small microchips present new challenges in their handling and mounting and in the creation of precise robust interconnects to them.

2.2 Large-Area and Plastic Electronics

Electronics may scale not only through miniaturization but also through the use of large-area manufacturing processes: Technologies developed originally for the manufacturing of flat-panel displays or X-ray sensors are being considered today for low-cost RFID circuits [17]. Depending on the application, polysilicon-on-oxide semiconductors with mobilities of 30 to 80 cm^2/V.s and organic semiconductors with mobilities of about 1 cm^2/V.s are interesting candidates for "good-enough" electronics. Alternatively, novel semiconductor materials such as nanotubes, graphene or nanocomposites are also emerging. Some of these material systems

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can be precisely deposited as inks, using a coating or printing process [18,19,20]. This opens up the exciting opportunity for the printing industry to participate in the manufacturing of larger-area devices such as electronic labels. Such labels are valuable for perishable goods or medicine and sit alongside barcodes and graphics on packaging. PARC has been developing libraries of analog and digital circuits [21] using gravure and flexographic techniques well familiar to the packaging industry [22]. Printed sensors, memory, batteries, and a few dozen transistors may provide sufficient intelligence to connect millions of packages of pharmaceuticals or food products at the edge of the IoE, at very low cost. Thinfilm Electronics, for example, has pioneered printed memory and sensor devices for brand protection and for monitoring the integrity of goods [23] (Figure 1.2.3). Xerox and Thinfilm recently announced a partnership for mass production and commercialization of cost-effective printed memory with cryptographic security labels.

The range and variety of sensor technologies required for smart labels and for the IoE in general is extremely broad. Electrochemical, optical, pressure, temperature, humidity, and many other sensors can be made printable and configurable for specific applications [24,25,26]. In many cases, printed sensors on plastic or paper substrates are ideal because they are low-cost and even disposable.

2.3 Printed Silicon-Plastic Hybrid Electronics

The performance of all-printed plastic transistors remains a limitation for certain smart-label applications, in particular where there is a need to implement complex communication protocols. Such networking protocols are needed to connect the smart everyday object to the IoE. The initial generation of smart printed sensor labels includes a display and is readable by humans, not by machines. This limits their applications. Implementing networking protocols are difficult due to the resolution offered by the printing process and the switching speed of the resulting transistors. Alternatively, a hybrid approach, involving printed sensors and interconnects alongside conventional ICs and other microelectronic components, combines the benefits of high-performance microchips with the flexibility of printing and it opens up unique innovation opportunities [27].

Flexible conformal electronics enables a new generation of wearable devices and of sensor systems. Soft and stretchable systems are key for prosthetics and soft robotic actuators. Electronics that are an integral part of cars, aerospace components or even buildings are often called structural electronics [28]; they combine micro with macro features and elevate integrated electronics to new large-scale levels.

The emerging field of flexible hybrid electronics (FHE) has recently been identified by the US Government as a critical area for investment. They awarded $75M for the creation of the Flexible Hybrid Manufacturing Innovation Institute (FHEMII). This Institute comprises 96 companies, 11 laboratories and non-profits, 42 universities, and 14 state and regional organizations, among them PARC [29]. The Institute will be led by the nonprofit US FlexTech Alliance, bringing together disparate industries for the creation of new manufacturing infrastructures for electronics. Key players including chipmakers, electronics assembly firms, printing companies, chemical companies as well as end users in the automotive, aerospace, medical fields, will be working together to create novel flexible hybrid electronics capabilities.

Examples of applications of FHE include wearable performance monitoring devices detecting stress levels from sweat and transmitting the data wirelessly. Such devices may take the form of an unobtrusive patch worn on the skin [30]. PARC and UC San Diego have been working on a personalized mouth guard that detects glucose in saliva [31]. Such performance monitoring devices are critical for safety of pilots, athletes, truck drivers among others. In collaboration with health professionals, these devices will be extended with further sensors to monitor a multitude of health-related conditions. Personalization and on-demand configuration is an important aspect of FHE devices. On-demand manufacturing will also enable the fabrication of electronics locally, for example on a ship or even a space station – the latter is an important goal for NASA's Jet Propulsion Laboratory [32]. Flexible integration also enables large-area smart skins on aircraft and cars. Boeing is exploring flexible circuit concepts on the surface of aircraft wings for damage control sensors [33]. In many of these applications FHE is about spreading high performance electronics functionality over large surfaces in a seamless way.

A difficult technology challenge for FHE is to combine integrated circuits and flexible or conformal substrates such as plastic or paper. For example, mechanical integration of rigid chips onto flexible substrates requires the use of compliant adhesives that prevent delamination upon bending, and electrical interconnects to the IC pads that resist cracking at the interface. Robust printable interconnect materials and techniques are needed that withstand mechanical and thermal stress [34]. ICs need to be designed with interconnects that make it easier to print them with inkjet or aerosol techniques. Many of these systems will initially utilize serial-data-transmission protocols to reduce the number of interconnects. Printing techniques will need to achieve micron accuracy to print conductive lines, ideally processed at low temperatures compatible with plastic substrates. The use of bare dice and engineered transitions between rigid and soft components is also a critical technology challenge to be resolved.

An example for FHE integration is a prototype wireless-strain-sensor sheet developed by PARC and shown in Figure 1.2.4. It consists of a flexible substrate with printed sensors, antenna, interconnects, combined with a silicon IC for analog-to-digital conversion, processing, and RF communication. This system monitors the input from two strain sensors that respond to bending. The system is operated by RF energy and is therefore battery free. A multitude of such self-contained sensors that harvest their own energy can be envisaged on a large-area surface such as the wing of a plane.

Power solutions based on energy harvesting or low-cost batteries will be essential components of smart IoE objects. Energy harvesting is very appealing since one has to consider potentially trillions of everyday objects being part of the IoE. Sources for energy harvesting may be the aforementioned RF, mechanical, or solar. Ultra-low power chip technologies with dedicated energy management for energy harvesting will be necessary for such large IoE networks [35]. Printable rechargeable batteries or super capacitors that can be shaped to the available space within objects will enable more power-hungry applications [36]. A couple years ago LG Chem for example announced curved and shaped batteries in production [37].

2.4 Future Outlook

The vast diversity of smart objects will require highly-flexible versatile manufacturing techniques to address all the emerging IoE applications. Printing has the potential as a digital on-demand integration technique to create systems with an arbitrary configuration of sensors, along with printed and discrete silicon electronics in new form factors. In recent years PARC has been exploring how to incorporate microchips or "chiplets" themselves into raw materials and use this as the ink for printing electronics [38]. Tiny chiplets, tens of microns across, can be dispersed in an ink similar to liquid toners used in conventional document printing. The chiplets are then guided to their destination using electrostatic forces, a technique similar to that used in conventional laser printing, as shown in Figure 1.2.5 [11]. Design sets comprised of small building-block circuits which mix Si, GaN, and other types of ''electronic inks'' enable complex heterogeneous systems, for example FPGAs. High-speed printing processes similar to xerographic processes or electrophotography have the potential to provide extremely high throughput. By combining various printing techniques and a broad set of materials, unique "application-specific" smart objects can be manufactured on demand.

Ultimately, everyday smart objects will become increasingly personalized. They will contain intelligent functions that were not previously possible. The additive 3D manufacturing of mechanical components is already an enabler not only for rapid on-demand prototyping, but also for manufacturing unique custom parts and for designing components with entirely new design rules. Commercial applications created with printers from 3DSystems, Stratasys and others are found in personalized healthcare, automotive, aerospace, education and many other fields. In general, the integration of electronics with the above 3D manufacturing techniques will create whole new design approaches for the creation of entirely new classes of individualized smart everyday objects, all connected to the IoE.

3. Information-Centric Networks

Today's Internet builds on the Internet Protocol (IP) which was designed to create a point-to-point network where *communication* happened between two end-points identified by their IP addresses. Exponential growth in video-on-demand, social media, e-commerce, and other mobile applications has converted the Internet into a *content-distribution* network putting stress on a system that was not designed for this purpose. The emergence of the IoE interconnecting billions of smart everyday objects that stream zettabytes (10^{21}) of structured and unstructured data (such as sounds, images, videos, and more) will strain the

current Internet even more. Also, an information search query in Google is different from gathering sensor information from an everyday object. The latter is equivalent to "Googling reality". For example, by using intelligent cameras and wearable devices it will be possible to remotely monitor most vital signs and diagnose a variety of diseases. "Googling" our elderly parent's temperature, respiration rate or heartbeat and predicting emergency events, even if they live on the other side of the world, will become possible. As expected, preserving an individual's privacy and protecting security are top priority requirements for any new network approach.

Novel networking protocols are being developed that will enable increased versatility, reduced Internet traffic congestion, and provide better data security. PARC is working through the IRTF (Internet Research Task Force) and with other companies to create an information-centric Internet protocol called Content-Centric Networking CCNx®. As a pioneer in network research, developing technologies like Ethernet in the 1970s [39], PARC over the past decade designed CCNx to take advantage of everything the Internet has to offer, including storage and data processing. Building an information-centric Internet architecture presents a number of challenges and opportunities for general-purpose and custom silicon-circuit designs, as will be shown here in this section.

3.1 Traditional Internet Limitations

The Internet is a wonderful tool that has allowed the rapid development of many industries by enabling communication and interaction that was previously not possible. However, it is not without its limitations. With its origin in the 1960s and mirrored to how a regular phone connection worked, the Internet is a product of its environment. It all started with a small number of connected computers, low bandwidth requirements, and the collaboration of a limited number of devices. The design choices made in these early days were not only appropriate, but also visionary. They have worked remarkably well for over half a century. There are however, a number of areas where the Internet now falls short: The three main ones are security, scalability, and versatility.

Security is a more recent issue: it has been bolted onto the current Internet. The two main protocols that run on the Internet, namely IP (Internet Protocol) and TCP (Transmission Control Protocol), have no inherent notion of security. They expect participants to be cooperative; either because security is provided by an underlying system (as in the case of the military) or because malice is rare (as in the academic case). Thus, in order for industry to thrive, extra layers of security protocols were created. While these do provide assurances, they have a cost in complexity, latency, and overhead. Hence, a built-in security framework would make networking much more resilient.

Scaling up is a challenge. Moore's and Nielsen's Laws predict exponential increases in computing and communication. We created Internet models and protocols that assumed a certain ratio of bandwidth and latency. These models no longer work since we have greatly increased bandwidth, without speeding up data packets, in view of the limitation of the speed of light. There are various solutions that try to address this, one of the most promising ones involves intermediate network routers taking an active part in the communication.

Versatility is essential for communication models that do not map to device to device data transfers such as the IoE where machines or objects communicate with each other. Internet protocols have evolved to tackle one main problem: directly communicating from one host to another. Other types of communication are not handled very well. When we must connect millions of sensors in the IoE, the Internet protocols starts to struggle: The model for two hosts negotiating a communication channel is very different from the model of millions of smart everyday objects sending data to a few collection points from where action is taken.

3.2 New information-Centric Internet

The networking community has tried to address the limitations of the current Internet architecture in various ways: Most proposals take an evolutionary approach, building on top of existing protocols. The more visionary proposals begin with a blank slate. In addition to the efforts by industry, several academic projects are being funded by the National Science Foundation under its Future Internet Architecture Project. The most advanced is the Named-Data Networking project led by UCLA which focuses on information-centric architecture and has its roots in PARC's original Content-Centric Networking CCNx protocol [40].

CCNx is a protocol designed from the ground up with the three shortfalls noted above in mind. It takes what we have learned so far in our 40 years of Internet experience and creates a modern protocol that will support the IoE. For example, in a traditional network your home gateway plays a very simple role of forwarding packets from the outside into your home. In CCNx, the gateway can help with the communication by caching packets (such as buffering a Netflix stream) when you have a weak WiFi signal so as to prevent communication interruptions. The schematic in Figure 1.2.6 shows the process that a CCNx gateway uses to request, receive, and store content.

While the standard IP protocol relies on specific source and destination addresses, CCNx is based on named requests and named data packets (Figure 1.2.7). Every piece of data in CCNx is named in a way that allows the network itself to find, move, store, and process it. CCNx can find the data in the nearest location where it is available and does not need to go to all the way to a source address. This minimizes network traffic and latency. Large files are chunked into small packet size pieces of data that are then named so the network can transfer them upon request. Named data is self-identifying and decouples the one-source-to-one-destination communication requirement from the network architecture. Nodes request data based on names and not endpoints. Any reachable element in the network that holds the data is able to answer the request.

Security is built from the ground up, on every piece of data and every request. Each piece of data is named and secured. Signatures guarantee data provenance, not the node that transmitted the data. This is a more secure approach to transmitting sensitive data. Network routers can help communication. By looking at the names being requested and transmitted, network routers can make choices about the traffic they are transferring. By observing the relationship of past requests they can predict future requests, store appropriate information, and manage resource utilization.

These properties of CCNx give the network a resilience that is far superior to those of today's Internet. It enables improved performance, lowers bandwidth requirements, and provides better resource utilization.

Using named data enables services to concentrate on the data they produce, not where it is or where it needs to go. For example, temperature sensors could create readings and name them with the location and time. Interested clients could then request this data based on specific names. If given the proper authorization, they could then take action automatically. No coordination is needed between the specific devices, simply an agreement in the way data is named. This technology is currently being evaluated by academic institutions for application to building-management systems [41], vehicular networking, real-time conferencing, and more.

3.3 Challenges for General-Purpose and Custom-Silicon Electronics

Naming every piece of data on the Internet, every current data packet and all future data packets, means that we need powerful hardware that can perform all required computations on names at line rates (the maximum speed at which a link can transfer information), over 100Gb/s. stretching the limitations of today's devices.

While in the past we only needed to parse and match IPv4 or IPv6 addresses (32 and 128 bits respectively) in real time; we now need hardware that is able to parse, sort, match, and summarize arbitrary-length structured names (potentially thousands of bits). Doing this at line rates of hundreds of gigabits per second is non-trivial. To make matters more complex, due to the request-response nature of CCNx and the way it routes, every CCNx packet modifies the data structure (updating the pending table in Figure 1.2.6) at every router [42]. Current IP does not need to do this as today there is no state that needs to be kept in routers on a per-packet basis.

Because CCNx allows every request to carry a restriction on what is a valid reply (such as the specific key of a valid signer), every node must have a way to potentially perform an elaborate computation on the data of the packet (such as verifying a signature). While not all these computations have to be done at line rate, they must be done with the lowest time delay possible.

Cisco, Huawei, Alcatel-Lucent, and other companies are experimenting with information-centric networking approaches and evaluating off-the-shelf hardware solutions for its implementation [43]. As information-centric networking technologies develop, demand for routers and especially processors that can handle not only the high-speed and complex processing but also store huge amounts of information is expected to grow.

4. Automated Real-Time Insights

Once everyday objects with embedded sensors are connected to an information-centric network, the largest benefit comes from generating automated real-time insights that lead to actual actions. Machine intelligence enables smart everyday objects to read, see, hear, decide, and act, based on vast amounts of sensory input. Being able to act on real-time insights will transform user experiences and enable the automation of time-consuming business processes.

Analyzing massive data streams imposes four unique challenges that will be addressed in this section: (a) efficiently processing data on an everyday object at the edge of a network in real-time, (b) selectively beaming exception-only data into a centralized cloud to perform more-sophisticated analytics, (c) performing computational analysis of sensitive data without privacy or security breaches, and (d) actively adapting the analytics models to new data sources in a cost-effective way. There is an opportunity to design low-cost low-power secure deep-learning chips that can analyze huge amounts of real-time data in a secure and low-power way.

4.1 Data Processing "At the Edge"

The IoE with its sensors embedded everywhere, will provide a wealth of data on everything from smoke alarms to automobiles, medical devices, and wearables. It demands a sea change in how the vast amounts of often unstructured data are to be processed and analyzed. In the future, the bulk of analytics will take place at or near the source of the sensor that generates the data. Already today, distributed energy and transportation infrastructures include systems that are performing real-time analytics "at the edge" such as in the wind turbine itself or in the car. Consumer-oriented sensor data generated by low-cost wearables, home or office devices can be sent to a local edge node such as a mobile device or home gateway, where the computation takes place. Computation at the edge instead of in a centralized cloud has several benefits: It reduces the response latency and decreases the network bandwidth requirements. Additionally, regulatory and privacy concerns are addressed as users have more control over their own data. Private data is beamed to a 3rd party cloud by exception only [44]. For instance, using visual analytics, a security camera would send data to the cloud by exception only, such as when a human enters the frame. Immediate action can then be taken. Technical progress still needs to be made to address the power consumption and especially the sleep and wake-up modes as well as the energy harvesting capabilities of individual sensors.

Xerox has been helping city officials to optimize the flow of people through an urban area by providing the analytics tools and capabilities that allow people to commute as efficiently and effectively as possible [45]. Instead of gathering data for analysis later on, traffic light cameras will analyze information as they collect it and make immediate decisions to detect incidents and improve the flow of vehicles (Figure 1.2.8). Roadside traffic sensors will measure traffic patterns, and smart-parking-space sensors will simplify finding space by communicating with other in-vehicle sensors. Xerox is a founding partner of the Mobility Transformation Center at the University of Michigan exploring how people and goods move more effectively while improving safety, reducing congestion, and conserving energy.

4.2 Privacy-Preserving Analytics

As individuals become increasingly reliant on intelligent, interconnected everyday objects, security issues are becoming an even more significant threat. In addition, users want to control their private data and decide on what to share, with whom to share, and when to share. Conducting accurate and valuable analytics on personal data while properly protecting the individual's privacy is not easy.

The traditional security solutions based on well-bounded network parameters, such as firewalls, local area networks, and specific-application security, that can not sufficiently tackle the challenges in the increasingly dynamic and unbounded IoE environment. The interconnected objects are everywhere and cannot always be contained and accessed within a firewall. Furthermore, any IoE object being added is another potential entry point for a hacker. A holistic approach is required that tracks and adapts according to an individual's privacy requirements. The entire data lifecycle from generation/collection to processing/analyzing, to storage must be secured. Figure 1.2.9 illustrates a system view of three major components in an IoE security and privacy solution. First, at the level of the IoE objects, on-chip or hardware embedded security is needed for authentication, access-control and encryption while collecting and processing data. Second, a scalable and intrinsically secure network communication protocol (such as CCNx) ensures the secure data transfer and privacy-preserving interactions among all entities in an IoE ecosystem. Third, at the user level, the personalized privacy goals need to be captured, tracked, and aligned with the purpose of the analytics. Information such as who is authorized to access what data, where data can be processed, and how insights are extracted and shared must be understood and automatically controlled [46].

Privacy-preserving analytics breaks the tension between maintaining privacy and the ability to create valuable insights from personal data. Current secure privacy schemes (such as anonymization and encryption) do not support analytics on the data. As a result, weaker schemes, such as data masking, are often used for analytics tasks. PARC has developed an analytics platform which allows data scientists to perform analytics on sensitive data without decrypting the sensitive data or knowing the underlying security and privacy access codes [47]. This analytics platform was applied to analyze healthcare data amassed through electronic medical records, from imaging equipment, wearables, and other devices. Being able to do privacy preserving analytics delivers better personalized care decisions of professionals and empowers patients to take a more active role in managing their health [48]. The healthcare domain has many compulsory regulations related to data privacy which were incorporated in the new platform.

4.3 Adaptive Machine Intelligence

Deep-learning models are the state-of-the-art for many machine-intelligence problems such as image recognition, video processing, speech analytics and language parsing (Figure 1.2.10). Using neural-network models with layers of artificial neurons and millions of parameters, deep-learning algorithms leverage advanced hardware capabilities and the abundance of gigantic datasets. Deep learning is a sub-field of machine learning. Conventional machine-learning methods need a huge amount of human-labeled data to train the system. This is expensive and time-consuming. Humans do not learn this way. When a child sees millions of images throughout her development, without being told the name of every object, she nevertheless learns the concept of objects, the concept of the 3D world, etc. Once grown, a human can easily learn to recognize new classes of objects.

Inspired by human biology, researchers are developing tools to pre-train a deep neural network with large quantities of labeled data (such as.ImageNet [49]), then recycling the pre-trained model for new tasks with far fewer labeled data [50]. This approach is often referred to as "transfer learning". It enables systems to adaptively learn a new analytics task in a cost-effective way. This type of learning is currently restricted to a narrow field of expertise such as face recognition or license plate recognition. Research is ongoing to enhance machine intelligence capability to also learn tasks in new domains such as human-mood detection based on facial expression, or moving-vehicle recognition to automatically improve road safety.

4.4 Challenges for Custom Silicon Chips

In recent years, companies have been exploring ways for moving machine learning from software only approaches into hardware (Figure 1.2.11). One method is to co-design the hardware and software to enable fast and scalable machine-learning analytics at low cost [51,52]. For instance, graphics processing units (GPU) are well-suited for number crunching and matrix/vector computation involved in deep-learning algorithms. Recent GPU-accelerated deep-learning methods have demonstrated orders-of-magnitude improvements in speeding up training models by reducing run times of weeks down to days [53]. Custom chips are emerging that implement deep-learning algorithms in a more-compact and power-efficient way. Examples include Baidu's embedded system for deep learning, and CogniVue's (recently acquired by Freescale) Opus processors optimized for computer vision.

An alternative approach is to create a completely new chip architecture that mimics the human brain and natively matches the structure of deep-learning algorithms. Initial results show that machine intelligence such as understanding images, videos, speech and natural languages can be achieved [54]. Examples include IBM's neuromorphic chip TrueNorth, and Qualcomm's cognitive-capable platform Zeroth. While these novel chips hold much promise, the research is still in its infancy and presents many challenges. For instance, a custom chip architecture can make a specific deep neural network that can compute specific tasks fast and accurately. However, it is difficult to build one custom chip that makes all machine intelligence powerful independent of the application domain.

Today, it remains costly to adapt a custom chip with a pre-trained deep-learning model to new data sets or new domains. For example, adapting systems that recognize faces in still images to detecting human activity in surveillance video streams is not a simple task. Many custom chip architectures are also not intuitive for software programmers to use and easy-to-use program APIs must be created.

5. Summary

The Internet of Everything is about to become ubiquitous, it will indeed be "all around us and reside into the background of our lives" as predicted over three decades ago. Three technologies will make the IoE possible: smart everyday objects, information-centric networks, and automated real-time insights. This paper highlighted the central role of electronics in each of these three pillars: (1) smart *everyday objects* that sense data everywhere will be created by printed hybrid logic and sensor circuits using organic inks and "inks" containing microchips; (2) *information-centric networks* that increase the Internet's versatility, reduce its traffic congestion, and improve security, will require novel hardware and software; and (3*)* the creation of *automated real-time insights* at the "edge" of the IoE network will require deep-learning chips and novel machine-intelligence software.

Many IoE chip design challenges such as unique formats (flexible, conformable, large area), extra-low-power chips that harvest their own energy, security, privacy, low cost, fast processing designed for deep adaptable learning, and more, will continue to demand fundamental research and offer numerous commercial opportunities for the semiconductor industry for years to come.

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Figure 1.2.1: Smart objects with embedded intelligence integrated in conformal, flexible form factors. Concepts developed by PARC and Smart Design.

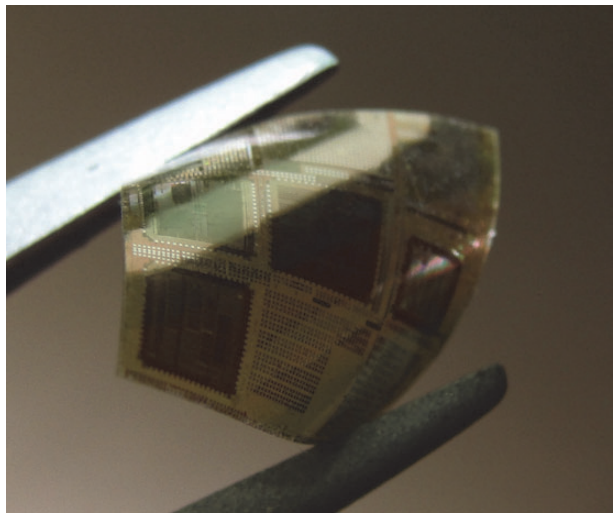


Figure 1.2.2: Flexible Silicon die with ultrathin microchips [15]. With permission from American Semiconductors.

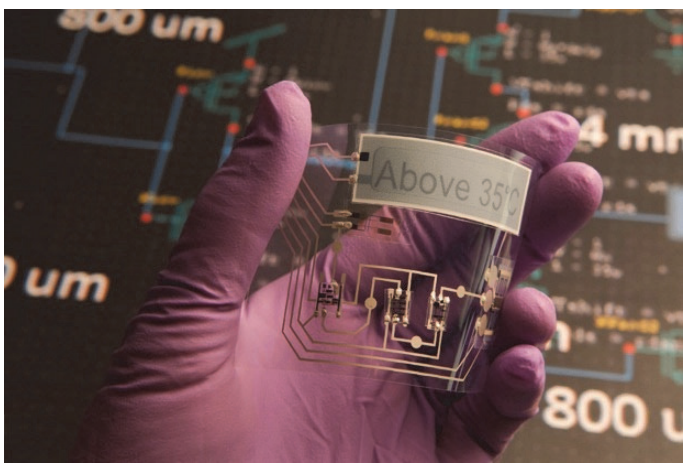


Figure 1.2.3: Printed temperature sensing label with memory, developed by Thinfilm Electronics and PARC [23] and partly funded by the FlexTech Alliance under US Army Research Lab Agreement W911NF-10-3-0001.

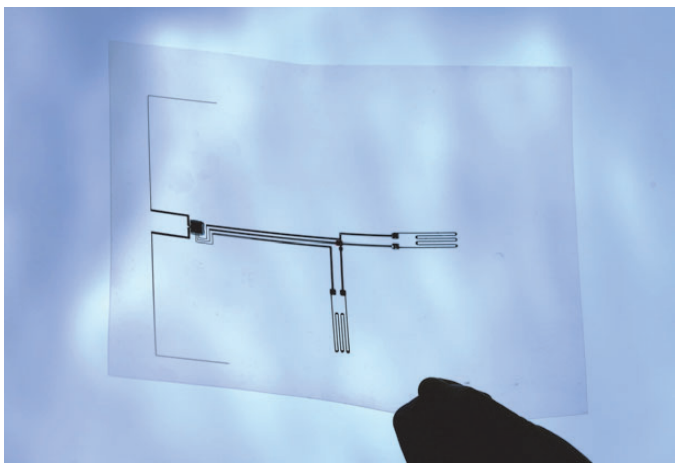


Figure 1.2.4: Printed hybrid wireless strain sensor sheet developed by PARC and funded by the FlexTech alliance under US Army Research Lab Agreement W911NF-10-3-0001.

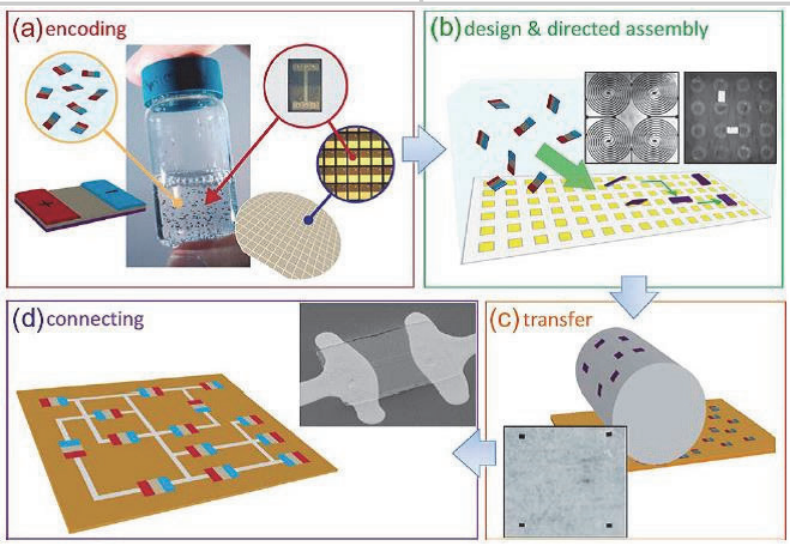


Figure 1.2.5: Four steps in the printing with microchip inks process [11]: a) chips are encoded with an electrostatic charge pattern to make inks, b) directed chip assembly using dynamic electric fields (fixed-pattern and programmable arrays shown), c) transfer to target surface, d) interconnects using ink-jet printing (insert).

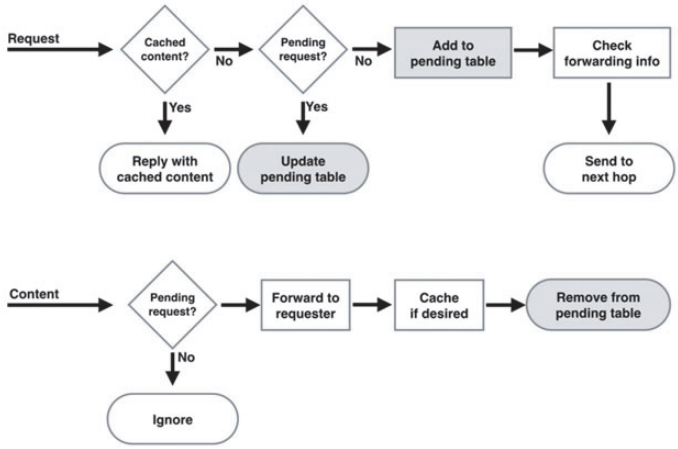


Figure 1.2.6: Process used by CCNx gateway to request and receive data. It helps recover from errors, saves bandwidth, increases security and lowers latency.

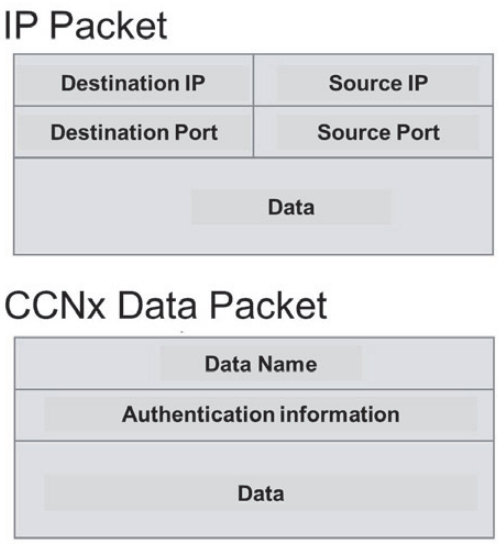


Figure 1.2.7: Internet Protocol Packet compared with CCNx Packet.

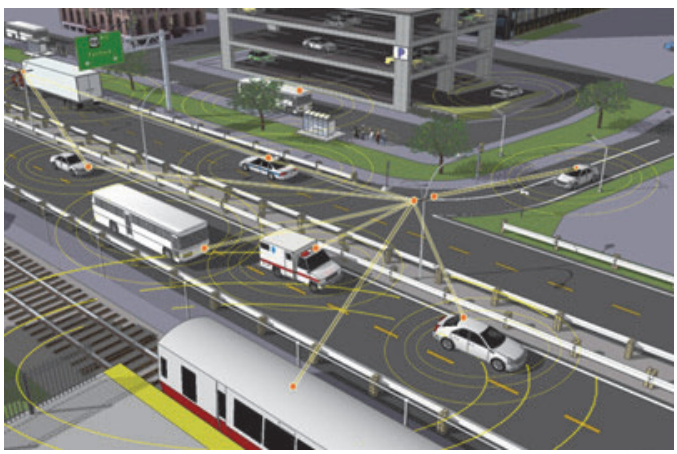
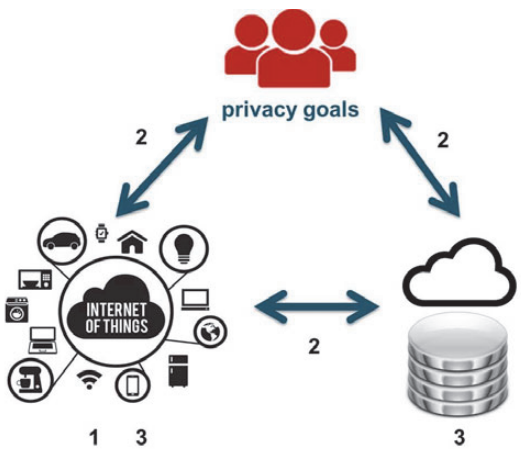


Figure 1.2.8: Smart Sensor Examples: multi-modality sensor information from vehicles and infrastructure is used for incident detection, safety, sustainability, and congestion mitigation (credit: US Department of Transportation).



1. Embedded authentication, access control & encryption
2. Scalable and secure communication protocols (e.g. CCNx)
3. Privacy-preserving data analytics

Figure 1.2.9: Three components in a secure IoE ecosystem.

Figure 1.2.10: Deep Learning and selected initial applications.

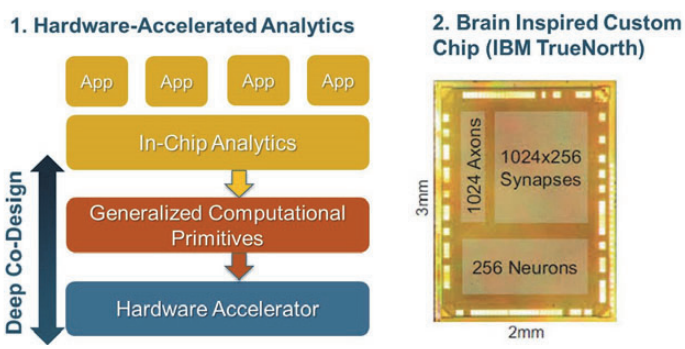


Figure 1.2.11: Silicon Chips for Machine Intelligence: Hardware-accelerated analytics and brain-inspired custom chips.

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Synopsys Macau and also with University of Macau, Macao, China

"For leadership in the analog circuit design industry"

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1.3 Evolution of 5G Mobile Technology Toward 2020 and Beyond

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1. Introduction

During the past few decades, mobile communications have significantly contributed to the economic and social development of both developed and developing countries. Today, mobile communications form an indispensable part of the daily lives of millions of people in the world; a situation which is expected to continue and become even more pronounced in the future. Mobile communication systems have the history of evolution from 1G analog cellular systems launched in 1979 to today's 4G LTE/LTE-Advanced. LTE was launched around 2010 and is now being deployed rapidly all over the world. LTE has become the mainstream of mobile technologies.

Overall, in the world market, a new-generation mobile communication system has been deployed almost every 10 years, as shown in Figure 1.3.1. Each generation tends to be used for a long time, and its peak, in terms of the number of subscribers, comes about 20 years after its initial launch [1]. For example, 2G GSM is still widely deployed in the market, worldwide. On the other hand, a different trend can be observed in the more-advanced market in Japan: As is typical, in advanced mobile communication markets, the peak of each generation comes earlier, about 10 years after the initial launch, as shown in Figure 1.3.2. This means that the number of subscribers and coverage area for each new-generation system has rapidly expanded, responding to advanced customer demand, with rapid migration from old technologies to new ones. Thus, in Japan, 1G and 2G were shut down 20 years after their launch, while for worldwide average, their peaks were just being reached! Notice that such an advanced market leads the technology to ultimately penetrate the worldwide market later.

Up to 4G, after the commercial launch of the previous generation, a concrete system concept and technology for the next generation emerged immediately. Thus, we saw 2G (TDMA: Time Division Multiple Access), 3G (CDMA: Code Division Multiple Access), and 4G (OFDMA: Orthogonal Frequency Division Multiple Access) systems as shown in Figure 1.3.3. In fact, there was a representative 4G technology (OFDMA) introduced in the early 2000s while no one wanted to use the term "4G" [2]. However, today, while everyone talks about 5G, there is no defined technology representing it. Thus, the current status of 5G is different from that of 4G ten years ago. This does not mean that there is no 5G technology, but rather that there are actually several candidate technologies for it. Of these, the OFDMA-based radio technology is still a major candidate. But, researchers in this area see some saturation in radio technology evolution since 4G radio access has almost achieved Shannon capacity at the link-level. However, innovative combinations of technologies will continue to create new technical solutions for the emerging new use cases. By such combinations, things which are considered impossible today will be achieved in the 5G era from 2020 and beyond. For example, the higher-frequency bands (above 6GHz), have been considered so far as not suitable for mobile communication systems. However, today, efficient use of higher-frequency bands is considered as one of the key components of 5G to provide a solution to the expected traffic explosion. The innovative combinations of technologies will provide cost-effective solutions for wide cellular coverage including the use of higher-frequency bands with broader bandwidths.

2. 5G Requirements

Taking into account recent market trends and services, high-level targets which are most relevant to 5G are summarized in Figure 1.3.4 and described in the following:

Higher system capacity – It is estimated that the volume of mobile traffic in 2020s will be at least 1000-fold larger compared to that in 2010. Thus, 5G must be able to manage traffic volumes which are many orders-of-magnitude larger than today's networks. This will be the most-challenging requirement for 5G mobile broadband.

Higher data rate – 5G must practically provide higher data rates than are deployed today. Also, considering the rapidly emerging trends to richer content and cloud services, 5G should target higher-data-rate services along with more uniform quality of user experience, compared to LTE.

Massive device connectivity – 5G must allow massive numbers of devices to be connected simultaneously to the network in order to support all-time connected cloud services even in a crowd of people, and more machine/appliance-based devices for the Internet of Everything (IoE), known also as Internet of Things (IoT).

Reduced latency – 5G must provide not only higher data rate, but also a user-plane latency of less than 1ms over the Radio Access Network (RAN), a large leap from the 5ms of LTE. In some specific cases, even 1ms end-to-end latency is declared to be needed. Lower latency will enable future cloud services and new potential services such as tactile Internet, augmented reality, and real-time and dynamic control for Machine-to-Machine (M2M) use cases.

Energy saving and cost reduction – 5G system must provide increased capacity per unit network cost and be energy-efficient and resilient to natural disasters. In particular, for M2M terminals, efficient energy saving is essential for achieving longer battery life (e.g., more than 10 years).

As shown in Figure 1.3.5, requirements such as higher capacity, higher data rate, energy saving, and lower network/terminal cost can be considered as traditional requirements for mobile communication systems up to 4G. Lower latency, however, is a relatively new requirement recognized from 4G that is currently a very important enabler of packet-based mobile Internet.

These targets will continue to be the eternal requirements for future mobile broadband. But, as well, some new requirements have emerged for 5G: For example, massive connectivity with extremely low power consumption is a new requirement to support IoE. Moreover, the flexibility to support new business models and ecosystems is being discussed actively. The collaboration with specializing verticals becomes important in expanding the business coverage to other industries beyond telecom.

3. Views on 5G and Beyond

From a technology perspective, 5G will include a new Radio Access Technology (RAT) and the evolution of 4G LTE, as explained later. It will also include evolved network architectures and core network technologies. On the other hand, from the mobile operators' business perspective, 5G is an end-to-end ecosystem which enables a fully mobile and connected society as stated in [3].

In 3G and 4G, the technologies came first with some doubts about the necessity of new-generation technologies at the time. Instead, the technology and its high performance created the demands and led to new services and businesses. However, for 5G, the discussion on business models came first and continues to overshadow consideration of technology, as shown in Figure 1.3.6. Thus, technologies will be created later in support of emerging ecosystems and businesses. This is quite an appropriate process for creating new technologies, but can be quite lengthy. This observation explains the difference between the status of 5G today and that of 4G ten years ago.

In our view, 5G will be launched in 2020 as shown in Figure 1.3.7. Even then, after its launch, 5G will continue to evolve. One example of this evolutionary process is 5G+: This transformation is similar to that of 4G where LTE evolved to LTE-Advanced. Thus, it is important to implement forward compatibility at the initial launch of 5G to ensure future evolution. 5G will be deployed initially in areas where higher performance is required, such as in urban areas around Olympic stadiums, possibly using existing frequency-bands, new bands licensed by 2019, and/or unlicensed bands. While, higher-frequency bands such as mm-Wave represent one key component to achieve extremely high performance, 5G is about more than higher frequency alone: 5G can be launched with other lower-frequency bands. Initial 5G will include some key radio technologies, such as massive MIMO, NOMA (Non-Orthogonal Multiple Access), and so on [4]. Technical components such as lean and low-latency radio design, in addition to numerology design to support a wider range of frequency bands, will be keys for future expandability. For existing bands, keeping backward compatibility is preferable, and thus the LTE evolution will be an important part of the 5G technology evolution. Beyond 2020, the deployment areas for 5G will be gradually expanded while introducing additional radio technologies and new higher-frequency bands.

5G will cover a wide variety of use cases: Mobile broadband, requiring very high performance; and massive M2M, requiring extremely long battery life. Furthermore, 5G will ultimately utilize a wide range of frequency bands including existing and new spectrum, which may extend to higher frequencies above 30GHz. Today, many technologies are used for various use cases in various

frequency bands. My dream is that 5G would cover all use cases within all frequency bands. Thus, 5G might consist of multiple components since it is difficult to have a single technology satisfy all requirements; however, it is beneficial to have a single consistent design philosophy for all of these components. But, in reality, by 2020 other technologies would be used for some use cases together with 5G, and interworking of 5G with these technologies may be required, as shown in Figure 1.3.8.

Technology convergence has been the general trend for cellular systems, as shown in Figure 1.3.9. Thus, in the 1G era, many different cellular systems were deployed, whereas today 4G LTE is the main technology trend. However, now, there are many other technologies for other use cases. My aspiration and ambition are to converge technologies for various use cases into a single technology centered around the cellular system. In fact, such trends have been already observed, for example in the case of Wireless Metropolitan Area Network adopting LTE-based technology. I would expect that such convergence would continue at least for the next 5 years, since examples of expanding the use cases are already seen in LTE standards (such as LTE-Broadcast, LTE-Unlicensed, Narrowband IoT, and so on). Technology convergence would be ideal, but divergence is likely to happen again in beyond 2020, for various reasons.

4. 5G Technology

As shown in Figure 1.3.10, there are two basic evolutionary paths that can be taken to support new system capabilities for 5G: The first is a step-by-step evolutionary path based on further LTE enhancements keeping the backward compatibility; and the second is a revolutionary path using a brand-new radio access technology (RAT) that may include major changes that are non-backward compatible with LTE. In our high-level concept, 5G will utilize a wider range of frequency bands with both frequency-optimized and frequency-agonistic (i.e., common to all frequency bands) radio technologies. In particular, new technologies for new spectrum bands can be non-backward compatible. Meanwhile, backward compatibility or allowing co-existence with LTE is preferable for frequency-agnostic new technologies when they are applied to the existing spectrum bands. Therefore, as shown in Figure 1.3.11, a promising way forward is that 5G radio access consists of enhanced LTE RAT and a new RAT, supporting the tight interworking between the two RATs via carrier aggregation (CA) or dual connectivity (DC). The new RAT may be introduced not only to the new frequency bands, but also to the existing frequency bands, although sufficient benefits need to be identified.

Moreover, a set of technical solutions is required in order to address future requirements and challenges. "The Cube" depicted in Figure 1.3.12 provides a holistic view of the main directions of the evolution for radio technologies. In what follows, we will present candidate solutions which address the 5G requirements along with each dimension of the Cube, that is network densification using small cells, improving spectrum efficiency with advanced radio technologies, and spectrum extension using a wide range of frequency bands.

4.1. Advanced C-RAN and Massive MIMO

Network densification using small cells with low-power nodes is effective in coping with the mobile-traffic explosion, especially in high-traffic areas; although the use of small cells themselves is an old idea. Meanwhile, CA is introduced as a feature of LTE-Advanced to increase the data rate. While CA itself is not particularly smart as a technology, but, rather, a "brute force" expansion of bandwidth using multiple component carriers, a combination of CA and small cells with Centralized or Cloud Radio Access Network (C-RAN), which we call "Advanced C-RAN" [5], will allow advanced new features. As shown in Figure 1.3.13, Advanced C-RAN adopts the centralized network architecture with many branches of remote radio equipment (RRE) and utilizes LTE-Advanced CA functionality between macro and small-cell carriers. This CA functionality helps to maintain the basic connectivity under the macro cell coverage, while small cells achieve higher throughput performance and larger capacity. The Advanced C-RAN architecture handles all processing for CA and mobility within one baseband unit (BBU), which drastically reduces the amount of signaling to the core network. In March 2015, Advanced C-RAN was introduced to provide LTE-Advanced services on DOCOMO's commercial network [5].

Innovative combinations, such as Advanced C-RAN, will also be important for 5G. For example, massive MIMO technology is a promising solution to exploit higher frequency bands [6] where there are more opportunities for wider bandwidths, and thus larger data rates. However, path-loss attenuation becomes more significant and coverage limited. As a result, some may tend to believe 5G is just a hot-spot system for complementary use. On the other hand, antenna elements can be miniaturized for higher frequency bands, and very large numbers of antenna elements can be co-located, thus forming very narrow beams. We expect such massive MIMO will become essential at higher frequencies since it will enable practical coverage for cellular systems while providing very-high capacity. However, a single technology does not provide a complete solution because massive MIMO does not operate before tracking the beam to the user equipment, thus, having some problems in providing stable operation as a system. Here, the combination of massive MIMO and macro-assisted small cells such as in Advanced C-RAN will provide the solution to achieve wide coverage even at high frequencies with extremely high capacity, extremely high data rates, and stable system operation, as shown in Figure 1.3.14.

Thousands of antenna elements will be required to achieve kilometer reach in bands over 10GHz. While the concept of massive MIMO is simply about increasing the number of antennas, and includes no other ideas, its implementation has many challenges and will be a key issue in 5G.

4.2. NOMA

It has become more challenging to improve spectrum efficiency in existing frequency bands. In particular, more-advanced designs are introduced in LTE/LTE-Advanced in order to further control/mitigate inter-cell interference, such as coordinated multi-point (CoMP) transmission and reception. To further boost spectrum efficiency, Non-Orthogonal Multiple Access (NOMA) is introduced as an intra-cell multi-user multiplexing scheme that utilizes a new domain that is the power domain, which is not sufficiently utilized in previous generations. In NOMA, as shown in Figure 1.3.15, non-orthogonalities are intentionally introduced via power-domain user multiplexing in one of the time or frequency or code domains. Easy user de-multiplexing and signal separation are enabled by the allocation of large power differences between paired users at the transmitter side and the application of Successive Interference Cancellation (SIC) or Maximum-Likelihood Detection (MLD) at the receiver side. As a result, both system capacity and user-throughput fairness can be improved for both downlinks and uplinks [7],[8]. Furthermore, NOMA is beneficial in supporting more simultaneous connections in either uplinks or downlinks, as needed to address the challenges of massive device connectivity.

NOMA relies on more-advanced receivers such as SIC and MLD, which require more processing capability in user devices and base stations. Therefore, the continuous evolution of processing capability of user devices (generally following Moore's Law), will remain essential particularly at lower frequencies. In fact, for inter-cell interference cancellation, Network-Assisted Interference Cancellation and Suppression (NAICS), including SIC was specified in LTE Release 12. Thus, in the future, more and more devices are expected to be equipped with more-advanced receivers.

4.3. Flexible Duplex

A frequency-separated macro/small-cell deployment, where various frequency bands are individually assigned to various cell layers, may use various duplex schemes, such as Frequency Division Duplex (FDD) and Time Division Duplex (TDD) for lower- and higher-frequency bands, respectively. Furthermore, full duplex (to allow simultaneous transmission and reception using the same carrier) may be realized in the 5G era. Therefore, it is desirable to support multi-band solutions such as CA and DC irrespective of the duplex schemes used in either the lower- or higher-frequency bands. In 5G, unlicensed spectrum bands (that is license-free mobile bands) should be also efficiently utilized by the superior radio technology of cellular systems. To this end, flexible duplex would support the joint operation of variable duplex schemes including FDD, TDD, one-way links (such as downlink/uplink only), and potential full duplex associated with opportunistic carrier selection for multiple bands including unlicensed bands.

5. 5G R&D Activities

At DOCOMO, we have started studies on 5G requirements, concept, and candidate technologies as early as 2010 [9]. Since 2012, we have been developing a real-time simulator to evaluate and demonstrate the 5G concept and the gains of candidate radio-access technologies with various setups and for various use cases. Figure 1.3.16 shows its"stadium" version, where a very large number of users are connected to the network.

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In December 2012, the world's first 10Gb/s data transmission was successfully tested in the field in an outdoor mobile environment using an 8×16 MIMO-OFDM transmission system with 400MHz bandwidth just at 11GHz [10]. We also developed a NOMA test-bed in order to confirm NOMA performance with a real SIC receiver, taking into account RF-hardware impairments [11]. Furthermore, we developed a channel sounder at 20GHz and a massive-array antenna with 256 elements, as shown in Figure 1.3.17.

Large-scale experimental trials of emerging 5G mobile technologies are also taking place in collaboration with world-leading mobile-technology vendors [12] to [14]. Overall, a wide range of technologies are under investigation over a wide range of frequencies. The trials include technologies such as radio interface design for lower latency, massive MIMO, dynamic TDD, new candidate waveforms, coordination of ultra-dense small cells, and so on.

6. Conclusion

Recently, LTE has become the mainstream of mobile technologies, and global expectations for 5G toward 2020 and beyond are rapidly growing. It is expected that 5G will cover a wide variety of use cases and a wide range of frequency bands. Today, some promising technologies are emerging, especially those using new technology combinations. Through such combinations, things which were considered impossible today will be achieved in the 5G era. Together, let us envision a new world: Wider coverage cellular systems even at higher frequencies, and single-RAT 5G system which covers all 5G use cases and spectrum bands.

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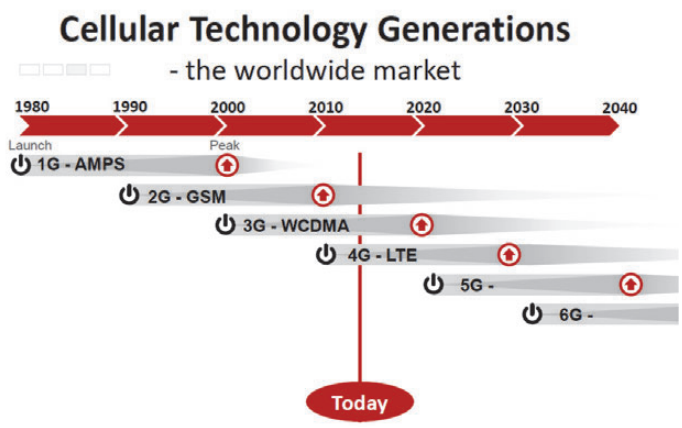

Figure 1.3.1: Cellular-technology generations in the worldwide market.

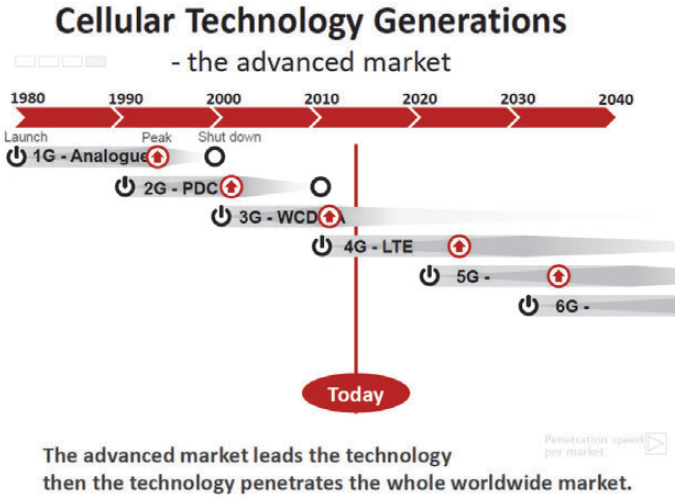

Figure 1.3.2: Cellular-technology generations in an advanced market.

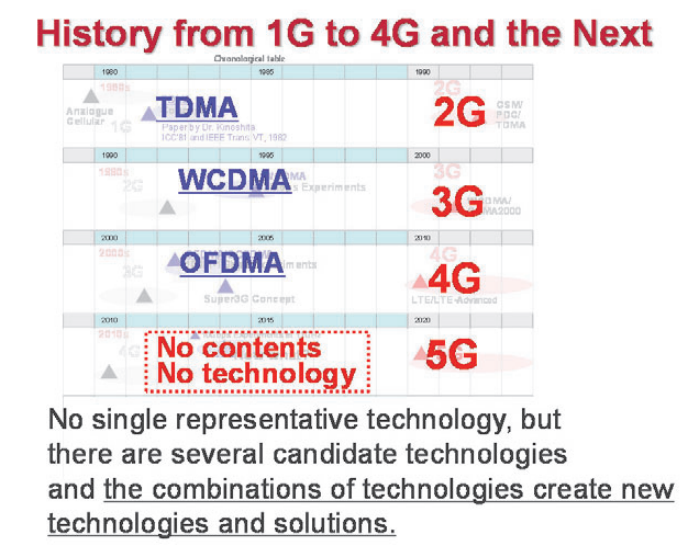

Figure 1.3.3: History from 1G to 4G and beyond.

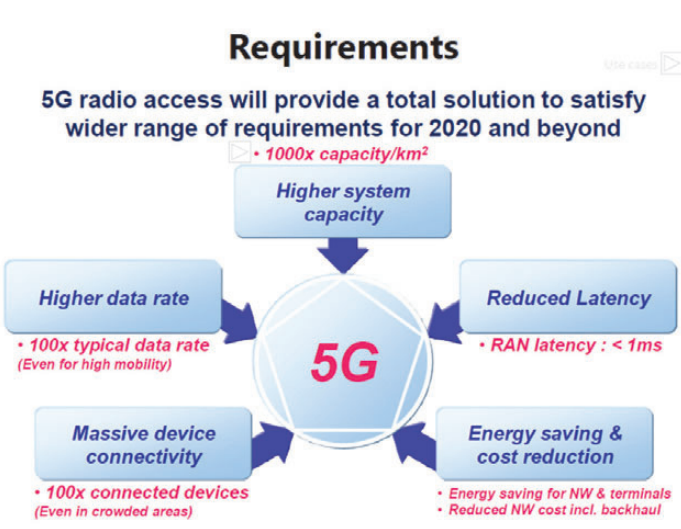

Figure 1.3.4: Requirements for 5G.

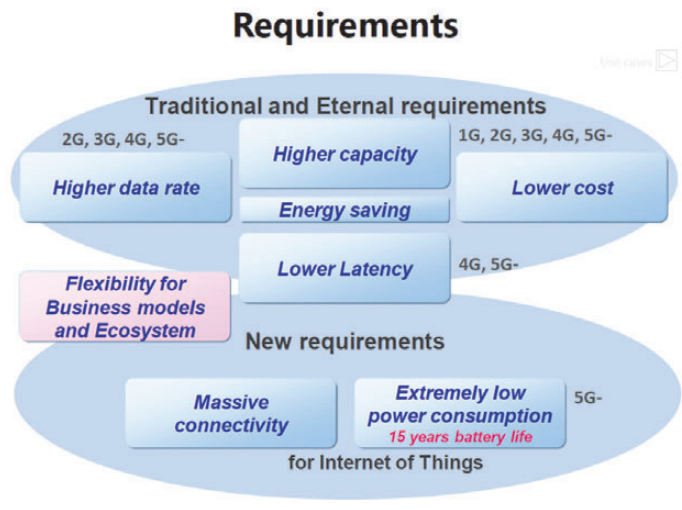

Figure 1.3.5: Trend of requirements in mobile communication systems.

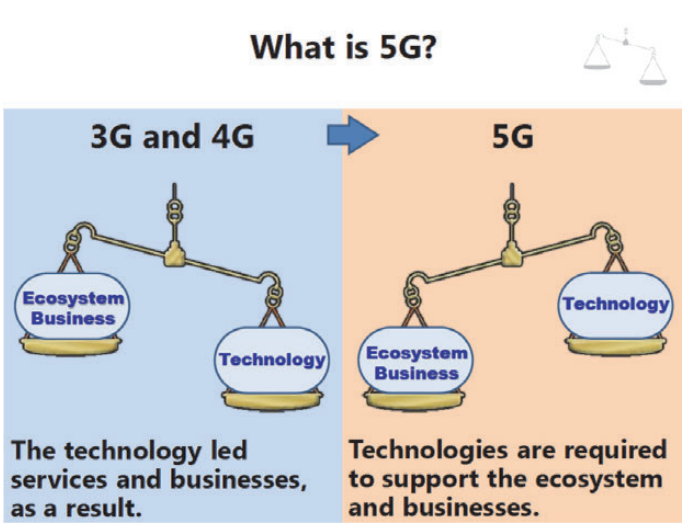

Figure 1.3.6: Relationship between business and technology over generations.

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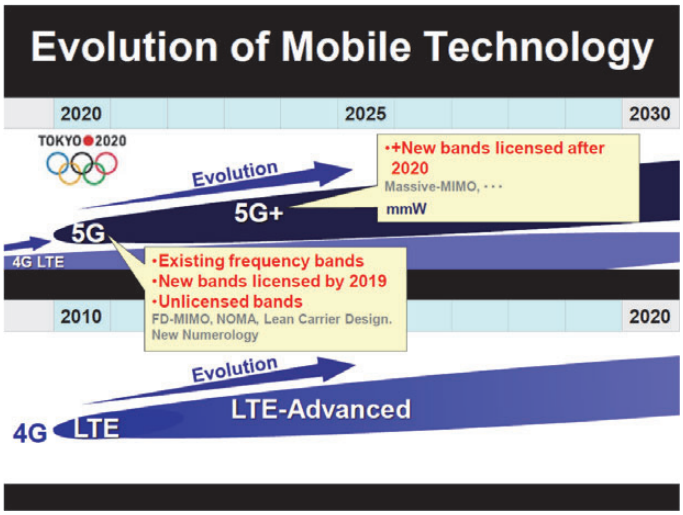

Figure 1.3.7: 5G time plan and its continuous evolution.

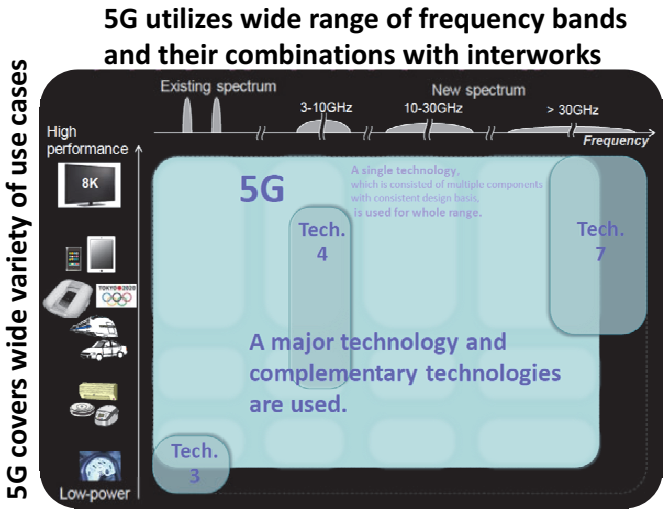

Figure 1.3.8: 5G technology covering a wide range of frequency bands and a variety of use cases.

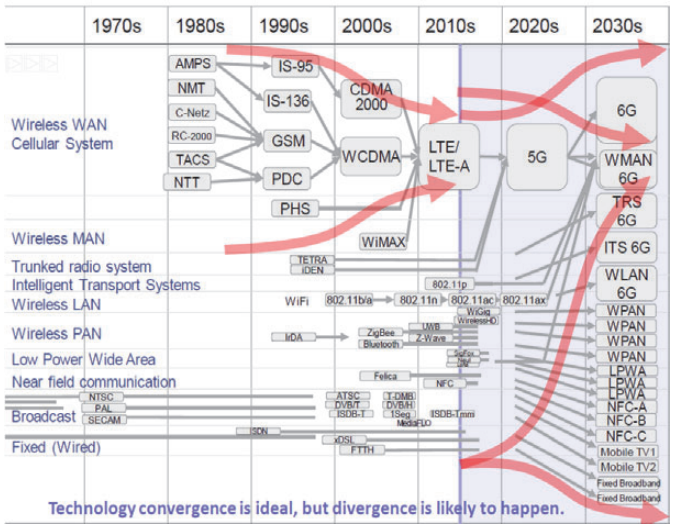

Figure 1.3.9: Technology convergence or divergence for 5G and beyond.

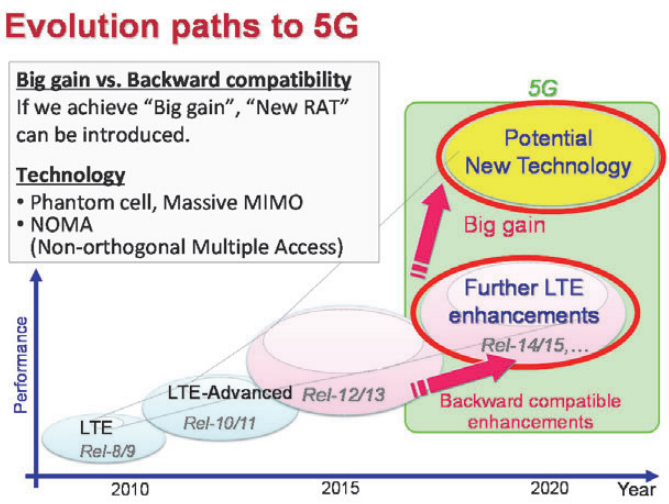

Figure 1.3.10: Evolution paths to 5G.

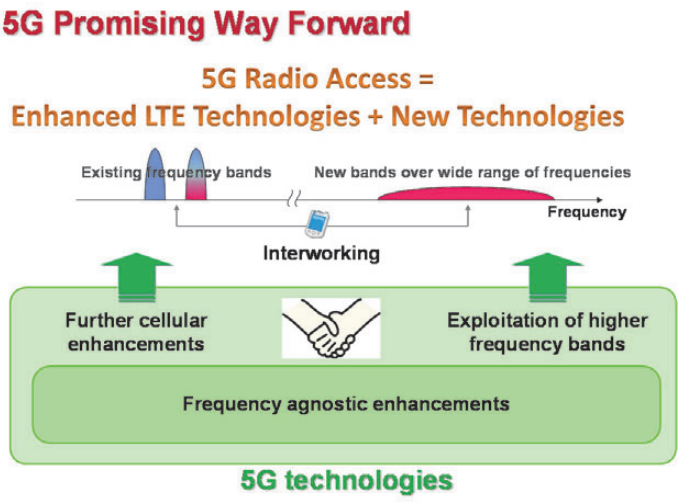

Figure 1.3.11: 5G promising way forward.

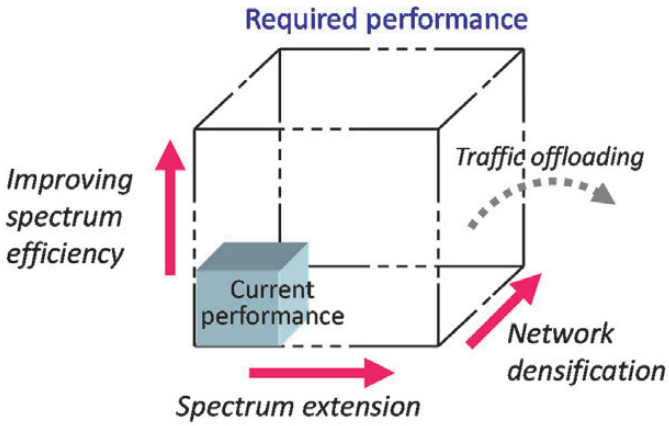

Figure 1.3.12: "Cube" to achieve 5G performance requirements.

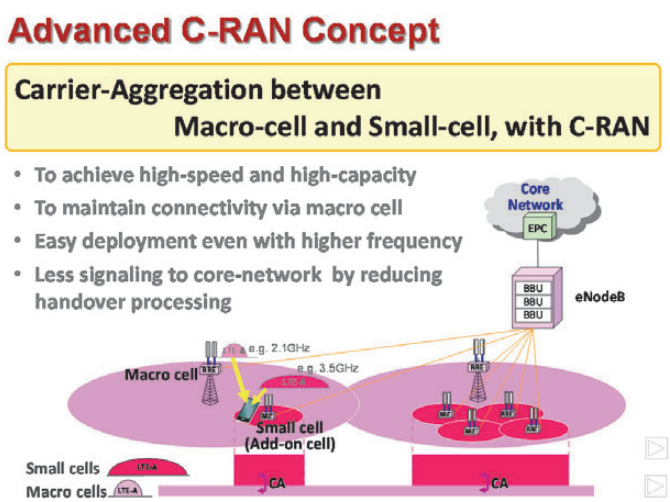

Figure 1.3.13: Advanced C-RAN concept.

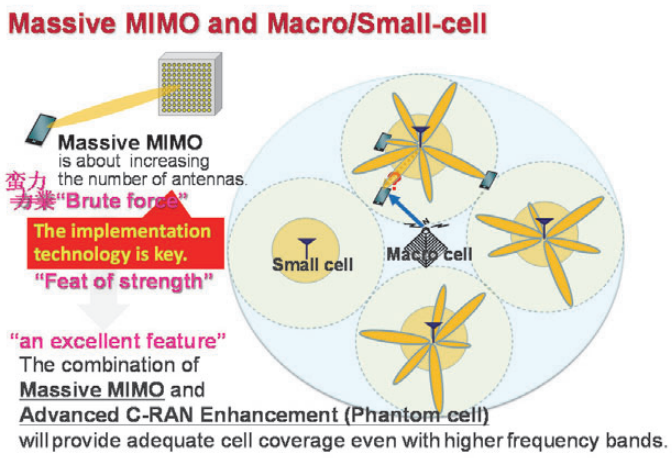

Figure 1.3.14: Massive MIMO and macro-assisted small cells.

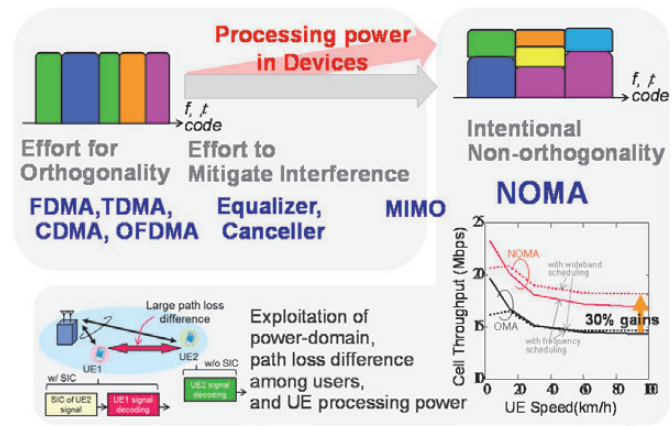

Figure 1.3.15: Non-orthogonal multiple access (NOMA).

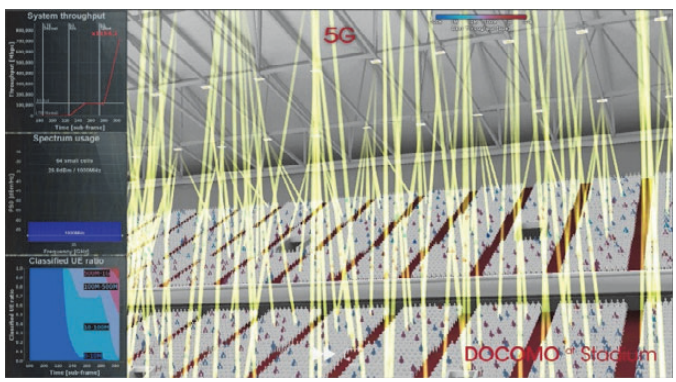

Figure 1.3.16: 5G real-time simulator (stadium version).

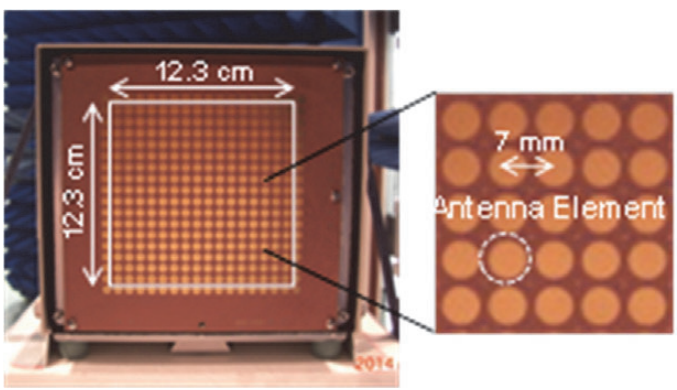

Figure 1.3.17: Massive antenna array used for channel measurement.

1.4 The Road Ahead for Securely-Connected Cars

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1. Introduction

The car as we know it is evolving. Thirty years ago the majority of innovations in the car were focused on the engine or body design, now 90 percent of car innovation is in electronics. Today, a typical car contains $799 of electronics (including $353 of semiconductors) which is expected to grow to $886 ($386) by 2022 [1]. Vehicles are transforming from simply a mode of transport to a mobile personalized information hub – they are enabling consumers to seamlessly integrate their mobile and wearable devices, and soon cars will also drive autonomously.

Advanced Driver-Assistance Systems (ADAS) enhance the safety of drivers and passengers and facilitates progressive driving automation (Figure 1.4.1). Enabling technologies to realize the fully-self-driving car includes secure vehicle-to-everything (V2X) communications, affordable compact radar solutions, and Ethernet for high-bandwidth in-car data transfer.

Self-driving cars will integrate a variety of wireless interfaces for the exchange of data with other vehicles and the surrounding intelligent traffic infrastructure – all aimed at understanding the world around it to optimize the traffic flow, reduce CO2 emissions, and avoid accidents. While being an essential part of autonomous driving, this connectivity also exposes cars to vulnerabilities such as hackers and viruses. Capable reliable wireless and wired communication technologies combined with powerful data-processing capabilities, at the highest levels of privacy and system security, are critical (Figure 1.4.2). This paper discusses what it takes to realize the securely connected car of the future.

2. Ethernet

Today, wired in-car communication is dominated by LIN (up to 20kb/s) [2], CAN (up to 1Mbs, with FD extended to 5Mbps) [3], and FlexRay (up to 10Mb/s) [4]. While the bandwidths are fairly limited, each of these standards is cost-effective for their specific applications. Furthermore, very stringent EMC and robustness requirements [5] need to be met to enable co-habitation with wireless systems and broadcast radio. Today, some high-bandwidth links are realized using dedicated point-to-point links typically utilizing shielded cables [6].

The gradual introduction of more electronic functions along with changes in system architectures with higher-bandwidth demands has necessitated a new network communication technology to avoid a steadily increasing amount of copper cabling in cars, implying extra cost and extra weight. Figure 1.4.3 illustrates the size of a typical cable-tree in cars today.

Higher-bandwidth-demanding applications include V2X, car radar, and other Advanced Driver-Assistance (ADAS) related functions, as well as advanced infotainment and high-speed wireless connectivity.

Automotive Ethernet is a new in-car point-to-point network communication technology based on a single Unshielded Twisted-Pair (UTP), initially at a simultaneous bi-directional speed of 100Mb/s, with an evolutionary bandwidth-increase path towards the future. Note that although Ethernet runs at a much higher rate, it must fulfil the same emission and similar robustness requirements as traditional in-car networks [7], leading to tough design challenges.

Automotive Ethernet can provide the necessary network backbone for autonomous driving and connected vehicles, because of its increased data capacity, cost efficiency, and weight reduction compared to existing solutions (Figure 1.4.4). It is expected that by 2023, 162 million Ethernet nodes containing 242 million ports will be included in consumer vehicles, worldwide (Figure 1.4.5).

Ethernet transceivers, switches and controllers enable a modular set-up, which allows automakers to build flexible and cost-efficient solutions for a wide range of networking architectures, from entry-level cars to high-end luxury vehicles. Ethernet will also pave the way for new distributed networking architectures required for autonomous driving and advanced infotainment systems. Some distributed digital signal processing close to sensors is desirable to realize an acceptable loading of the network.

Deterministic communication is vital in applications such as autonomous driving, where operational efficiency and functional safety are key. Deterministic Ethernet ensures high reliability in networked control systems, as well as high availability in fail-operational applications where continued operation is required in the event of control system failures (until the moment that the driver can take back control). It involves several additional standards including Time-Triggered Ethernet (SAE AS6802) [8], Audio-Video Bridging (AVB) [9], and Time-Sensitive Networking (TSN) [10].

This 100Mb/s (100BASE-T1) [11] is only the beginning for automotive Ethernet. Increasingly-sophisticated applications will continue to require higher bandwidths. Currently, an automotive-suitable simultaneous-bi-directional gigabit Ethernet PHY via a single UTP channel is being defined and IEEE standardized by the Reduced-Twisted-Pair Gigabit-Ethernet (RTPGE) Group and is expected to be released in 2016 as 1000BASE-T1 [12]. Semiconductor companies such as NXP are involved in standardization and are actively driving these changes in the ecosystem.

Object detection will be one of the prime applications for Gigabit Ethernet, since it requires higher bandwidth to transport (uncompressed) video. A modular system structure facilitates Ethernet-enabled cars to upgrade straightforwardly to higher bandwidth.

In the far future, bandwidth demand will undoubtedly surpass even the capabilities of automotive Gigabit Ethernet. Tough EMC requirements will remain key due to switching power-electronics in the car, and an increasing number of wireless systems inside and around the car. Potentially, new directions need to be explored for that, such as mmWave-through-fiber technology [13]. Academic research and collaboration with industry will be desirable in these explorations.

3. Vehicle-to-Everything (V2X) Communications

Vehicle-to-everything (V2X) technology involves exchange of vehicle and traffic information between cars and with the infrastructure [14]. Examples of typical V2X messages are warnings about hazardous locations, slow or stationary vehicles, emergency braking, emergency vehicles, road works, or the time and phase of traffic lights. Figure 1.4.6 shows an example situation. Automobile producers all over the world have recognized the huge potential of V2X technology for avoiding road accidents, improving the flow of traffic, reducing CO_2 emissions, and enabling autonomous driving.

V2X communications motivated a new IEEE 802.11p standard [15], a derivative of 802.11 as used in consumer Wi-Fi products. The IEEE 802.11p meets the stringent requirements of the automotive industry for Intelligent-Transport-Systems (ITS) applications, such as very low latency (<1msec), reliable non-line-of-sight communication, even under highly mobile channel conditions. V2X includes data exchange between high-speed vehicles and between the vehicles and roadside infrastructure utilizing the licensed 5.9GHz (5.85 to 5.925GHz) ITS band [14].

Field trials such as SPITS (Netherlands) [16], SimTD (Germany) [17], Score@F (France) [18], and Safety Pilot (USA) [19] underscore the positive impact that the technology can have. V2X has shown that it is ready to be used on the road: The results of simTD field trials involved 120 test vehicles that drove a total of 1,650,000 kilometres in 41,000 hours.

One of the important challenges is the penetration level of V2X in vehicles and in road-side elements. In order to have an effective network of connected cars, at least 10% of all cars must be equipped with an ITS module. This is especially difficult to achieve as various communication standards co-exist across the world. One effective solution is Software-Defined Radio (SDR). SDR can address regional differences in an efficient manner and matches the varying demands of global carmakers from low- to high-end car models.

It is expected that besides cars, vulnerable road users like pedestrians and cyclists will also benefit from V2X technology, enabled by low-power implementations. First solutions are underway; they combine communication between RFID chips in helmets or schoolbags with intelligent V2X capable traffic infrastructure [20].

4. Car Radar

Adoption of Advanced Driving-Assistance Systems (ADAS) will strongly increase in coming years. This trend is fueled by the improved affordability of these technologies, as well as by NCAP (New Car Assessment Program) which

demands autonomous emergency braking and pedestrian-protection systems for car makers striving for a five-star rating. Automotive radar is a key element in ADAS (figure 1.4.7), as it directly provides range, velocity and angular target information, complementary to other sensors such as cameras and LiDARs. For easy adoption and adaptation into a wide range of vehicles, small size and low cost are key market drivers along with the required high performance levels. In addition, low power also becomes of prime importance, due to reduced sensor size and high-ambient-temperature conditions. The radar IC is required to cover the extended 76 to 81GHz band for high range resolution. Recent results prove feasibility and suitability of RFCMOS radars for operation in the mmWave band [21], and open the way towards single-chip automotive-radar SoCs, including front-end and baseband processors on a monolithic die.

5. Near-Field Communication (NFC)

NFC [22] is rapidly emerging in the automotive market, driven by services like car sharing, corporate fleet management, Bluetooth and Wi-Fi pairing, and the demand for personalization inside the car. Combined with NFC-enabled car keys, wearables, smartphones or other portables, this technology can also be utilized for car access and engine start.

Automotive NFC can connect vehicles and car keys to portable devices and infrastructure, opening up the possibility for a broad range of connectivity innovations, for example payment services or connected displays. An essential requirement is that all three NFC operation modes are supported: Read/Write (Card Reader), Card Emulation (behave as Card), and Peer-to-Peer communication (device-to-device).

Applying the NFC Controller Interface (NCI) [23], NFC solutions provide interoperability with other NFC components to save development time and ultimately enable faster Time-to-Market of NFC-enabled applications for car OEMs.

6. Ultra-Wideband (UWB) Ranging

Ranging is already used today for distance bounding in Passive Keyless Entry (PKE) systems to determine the proximity and location of the car key or fob. A 125kHz signal is transmitted from multiple antennas in and around the car to wake up the key, and provide information about distance between the key and the car by measuring signal strength at the key site. Identification is handled by a successive RF (>300MHz) ISM band transmission, to open or lock the car. Thanks to multiple antennas, the key can also determine if it is inside or outside the car, or close to which door.

The new IEEE 802.15.4a standard [24] defines an alternative ranging technique by measuring the Time-of-Flight (ToF) of an Ultra-Wideband (UWB) RF signal between the transmitter and the receiver. UWB is especially suitable for this, as the ToF accuracy is proportional to the used signal bandwidth, while RF frequencies are sufficiently low to obtain the targeted range and enable a low-power car key implementation. Because UWB frequencies (3.1-10.6 GHz) are much higher than 125kHz, completely different antenna concepts can be used, providing additional degrees of freedom in the application. The UWB signal consists of narrow pulses, typically no more than 2ns wide with a bandwidth between 500MHz and 1.35GHz, making it robust against multi-path problems and interference. Besides supporting PKE systems, UWB ToF techniques can also be used for convenience functions such as user-approach detection and tracking, or wireless control of roof/window or mirror adjustment. It can also be used for extra safety with distance bounding for remote parking, to stop the car if the key and therefore the driver is too far away for proper supervision.

7. Security

The increasing number of electronic functions in the car brings great benefits to the driver, such as increased comfort, convenience, personal safety, and efficiency, but this comes with new risks. Modern vehicles are gradually turning into "smartphones-on-wheels" which continuously generate, process, store, and exchange large amounts of data. Wireless interfaces connect the in-vehicle systems to external networks, including V2X and cellular Internet, enhancing consumer experiences by enabling new features and services. But at same time, this also opens the door for hackers, making the vehicle vulnerable to cyber-attacks.

Several studies have already warned some years ago that hacking into a car is possible [25, 26], and more recently, researchers have demonstrated that they could gain remote control over vehicles [27, 27]. Therefore, steps must be taken now to secure the Connected Car and its wireless interfaces, to guarantee correct functioning of all in-vehicle systems, as well as user privacy.

In order to do so, security must become part of the entire lifecycle of the vehicle: Security must become an integral part of the design process, as opposed to an afterthought. This calls for security-by-design and privacy-by-design, which will have a significant impact on the in-vehicle electronics architecture. For example, safety-critical systems may need to be isolated from in-car entertainment systems by putting them into different physical networks. Furthermore, the security architecture, consisting of software and hardware, may need to be updated regularly during the lifetime of a car (typically 15 years), to remain on par with attacks which will get more severe over time.

The vehicle's security architecture shall be based on a defense-in-depth strategy, meaning that multiple security techniques are implemented across the vehicle's electronic architecture, to mitigate the risk of one component of the defense being compromised or circumvented. First of all, the car's external interfaces shall be protected, because they impose the biggest risk to the Connected Car as they open the door for *remote* and *scalable* attacks [27, 28]. These communication channels need to be protected against data theft and data manipulation, and unauthorized access via these interfaces to the in-vehicle electronics must be prevented. But, a second line of defense must be implemented in the in-vehicle network that connects all the various Electronic Control Units (ECUs), to protect against data theft, message and network manipulation, and inside-attacks where one compromised ECU is used to attack other ECUs within the vehicle's network. Finally, the ECUs themselves must be protected against software manipulation, privilege escalation, and so.

To provide protection at all these layers, well-known cryptographic technologies can be used, including data encryption and authentication of devices and messages. Additionally, the automotive industry must embrace security solutions that are already widely applied in smartphones and IT infrastructures, but are new to the automotive world, such as firewalls, intrusion detection and prevention systems, virtualization technologies, and secure firmware updates.

In general, securing systems with software only is not sufficient. At the very least, the security implementation needs to be isolated from other non-secure code, for example by executing it at a higher privilege level (system vs. user mode), enforced by hardware, or by implementing it in dedicated hardware. To protect against side-channel attacks, hardware may additionally need to be designed in such a way that it does not leak unintended information via timing, power consumption or electromagnetic leaks, which could be exploited by an attacker to find out what the hardware is doing, or what secrets are stored in it [29,30]. Lastly, physical attacks require physical protection: when hackers directly attack individual ECUs and ICs, physical tamper-resistance is needed to detect such attacks. For example, one can use integrated sensors (Figure 1.4.8), and upon detection, take appropriate countermeasures, such as powering off, or eventually even destroying critical data, to prevent that it cannot be stolen.

Key elements of secure systems includes hardware such as "roots of trust" or "trust anchors" which contain and protect specific data against attacks. These trust anchors are tamper-resistant small crypto-chips which are also used today in products like banking cards, passports, and health cards. As such, the Automotive industry does not need to start from scratch, but can leverage solutions and know-how that is readily available in these industries. The same technology can for example be used to optimally protect data transfer between connected cars and to verify who can have access to the infrastructure.

8. Automotive Quality

Devices developed for automotive applications must meet much higher standards than devices in the consumer industry. Devices in cars must withstand harsh environmental conditions, such as a wide temperature range and mechanical stress, and must meet automotive EMC requirements. Furthermore, reliability and lifetime constraints are much more stringent, as illustrated in Figure 1.4.9.

Therefore, meeting automotive requirements necessitates a different way-of-working and requires stringent control of process technologies, packaging, circuit design, and product-development.

In order to realize our zero-defect vision, many automotive specific measures, constraints, and methods must be applied to automotive circuit design. This includes design for 100% test coverage, and stricter rules on device size, metal

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width and spacing, layer densities, number of contacts (Design for Manufacturability). As a side effect, this typically leads to larger designs consuming more power in order to meet these robustness requirements. These methods, while not fully eliminating, largely mitigate the risk of failures in vehicles. These design constraints are complemented by closely controlled production management, extensive testing and reliability stresses and strict change management. On top of that, there are also increasingly high expectations regarding failure analysis, traceability, audit, fab and sub-supplier management, product life cycles, and availability expectations.

9. Summary

Large-scale proliferation of self-driving fully-connected cars will only materialize if they are secure and reliable. Automotive quality and security are essential to ensure consumer confidence in these new technologies. Key functions needed to enable autonomous driving like V2X, car radar, and Ethernet become already available today but will continue to evolve in performance as well as integration level. Advanced mixed-signal RFCMOS technology enables the integration of high-performance wireless functionality, together with digital signal processing at low power and low cost.

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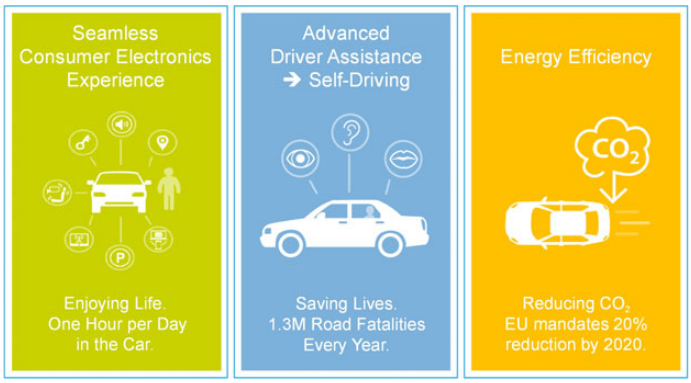

Figure 1.4.1: Trends Driving Automotive Innovation.

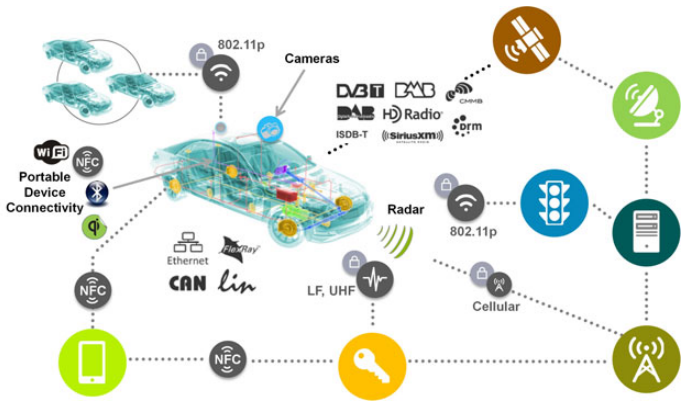

Figure 1.4.2: Communications inside and around the car.

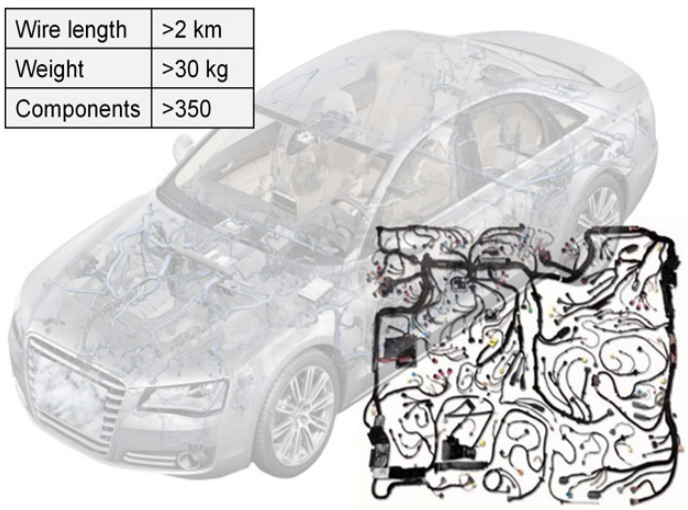

Figure 1.4.3: Cable Tree in a Car.

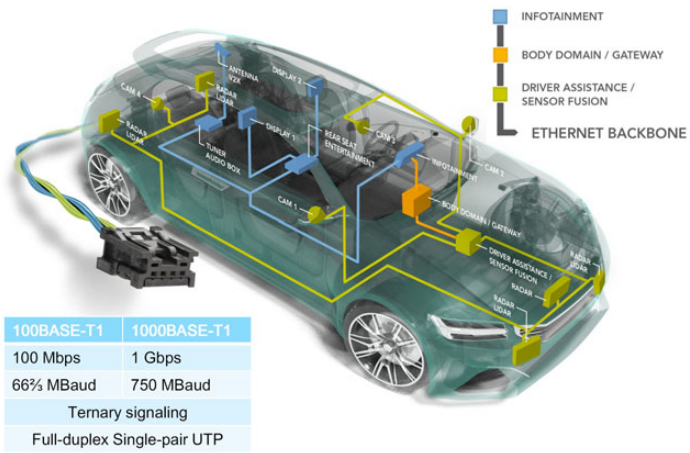

Figure 1.4.4: The Ethernet Backbone in a Car.

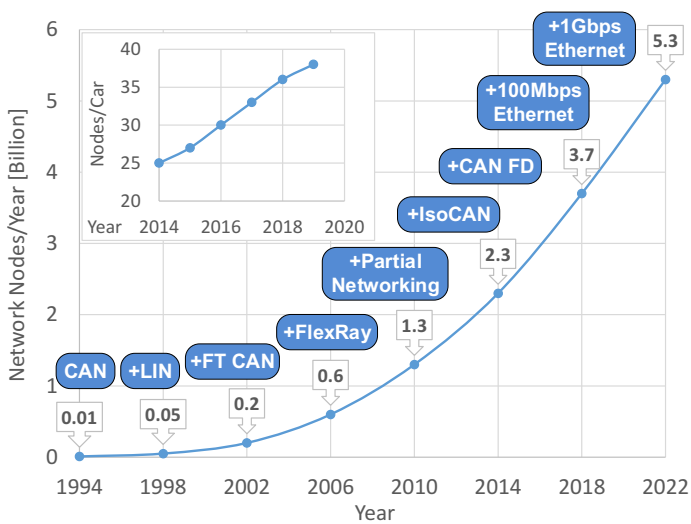

Figure 1.4.5: Projected Growth in Automotive Wireline Nodes.

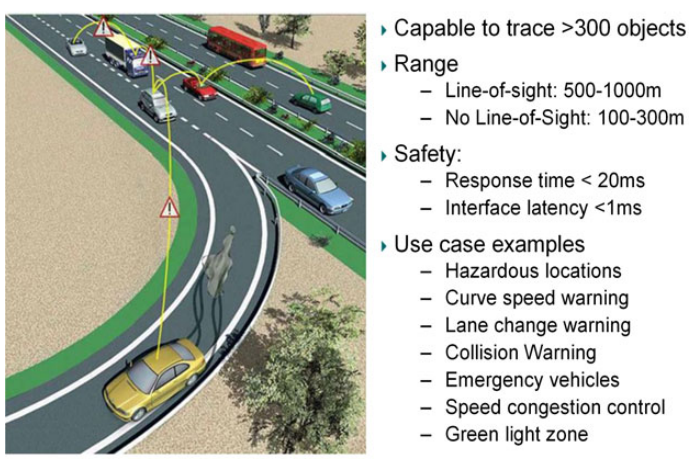

Figure 1.4.6: V2X in Action.

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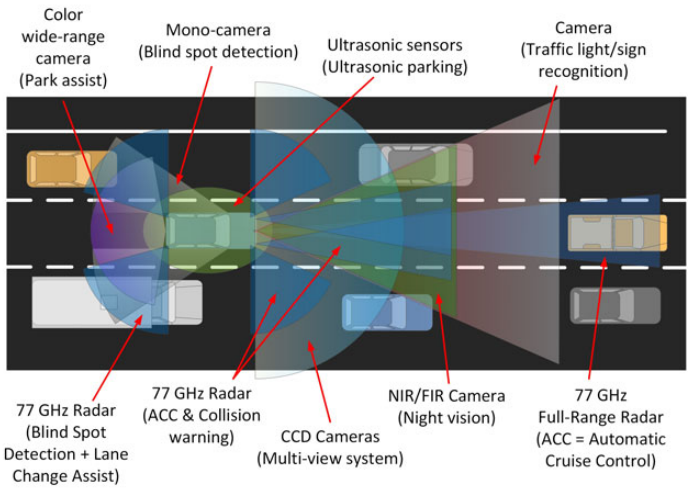

Figure 1.4.7: Sensor Fusion.

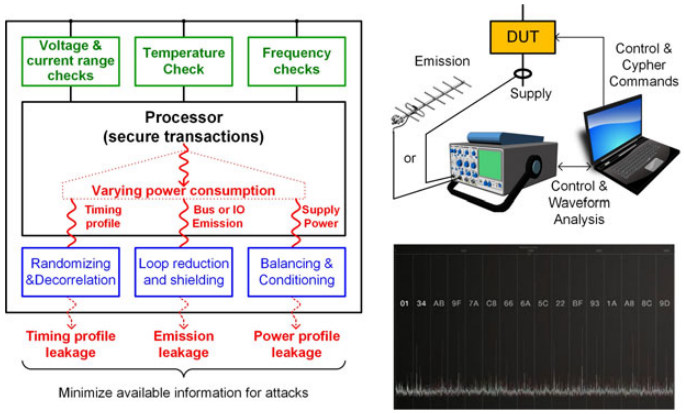

Figure 1.4.8: Physical Attacks and Hardware Protection.

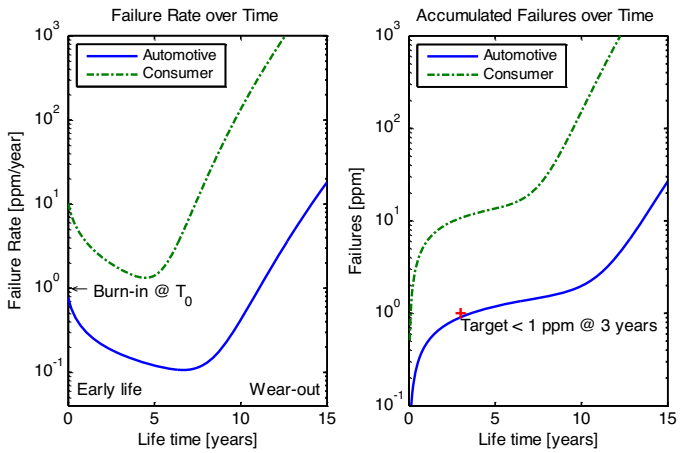

Figure 1.4.9: Reliability Comparison: Automotive vs Consumer Products.